Derivation of Interconnect Length Distribution in X Architecture LSIs

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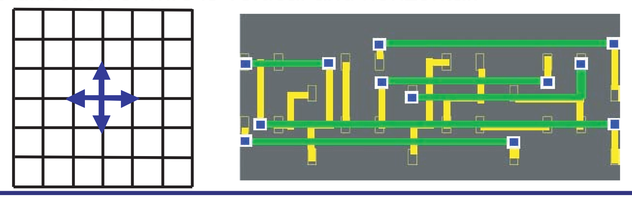
Interconnects Length Distribution (ILD)
ILD shows relationship between interconnect length and the number of interconnects.

→ Estimation of power consumption, clock frequency, and chip size.

→
- Evaluation of a chip
- Optimization of interconnect layout

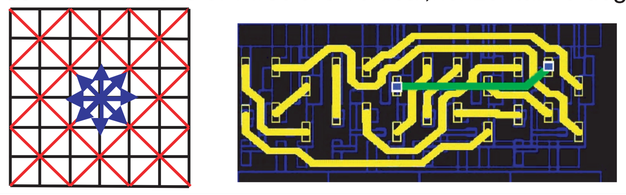
1. X Architecture

Standard: The direction of wire is vertical and horizontal.



Reduce
# of vias, and
Interconnect length

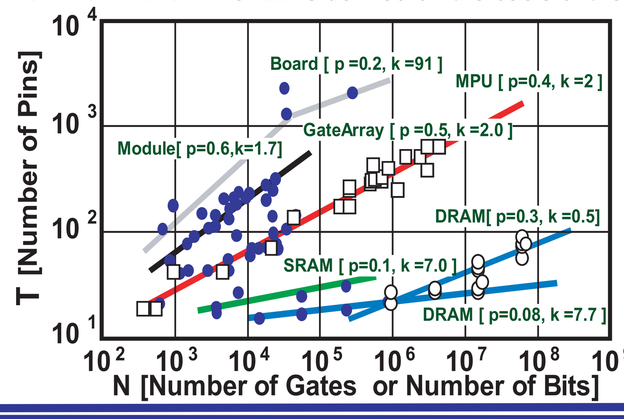
X Architecture: The directions of wires are vertical,horizontal 45 degrees.



X initiative : http://www.xinitiative.org/wt/home_flash.php

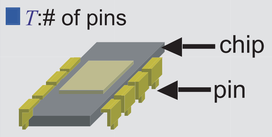
2. Rent's Rule

The ILD is derived on the basis of the empirical Rent's rule.



Rent's rule : $T=kN^p$

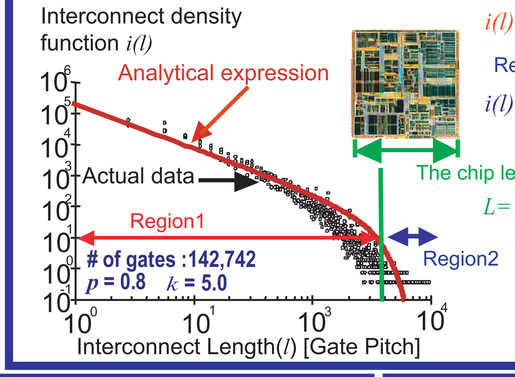
- T:# of pins



- N:# of logic block
- k (Rent's constant)
  :average # of ports of gates
- p (Rent's constant)
  :the complexity of circuits

3. Analytical Expression of ILD

Interconnect density function $i(l)$



The chip length of one side is $\sqrt{N}$
$L=\sqrt{N}=377$

Region1: $1\le l<\sqrt{N}$

$$i(l)=\frac{\alpha k}{2}\Gamma\left(\frac{l^3}{3}-\sqrt{2}Nl^2+2Nl\right)l^{2p-4} \quad (1)$$

Region2: $\sqrt{N}\le l<\sqrt{N}$

$$i(l)=\frac{\alpha k}{6}\Gamma\left(2\sqrt{N}-l\right)^3 l^{2p-4} \quad (2)$$

$$\Gamma=\frac{2N(1-N^{p-1})}{-N^p\frac{1+2p-2^{2p-1}}{p(2p-1)(p-1)(2p-3)}-\frac{1}{6p}\frac{2\sqrt{N}}{2p-1}-\frac{N}{p-1}}$$

$$\alpha=\frac{f.o.}{f.o.+1}$$

- Analytical expression shows the relation interconnect length and the number of interconnects

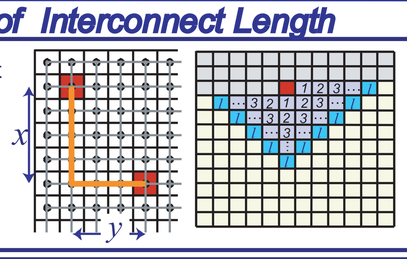
J.A.Davis,V.K.De,and J.D. Mindl:IEEE Trans. Electron Devices.45(1998).580-589

$i(l)$:# of interconnects
k&p:Rent's constants
$f.o.$:average fanout
N:# of gates

4. The Calculation of Interconnect Length

Orthogonal interconnect

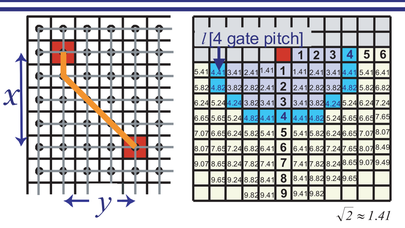
$L=x+y$



Diagonal interconnect
(X Architecture)
Using computer simulation

$L=(x-y)+y\sqrt{2}$ $(x\ge y)$

$L=(y-x)+x\sqrt{2}$ $(y>x)$

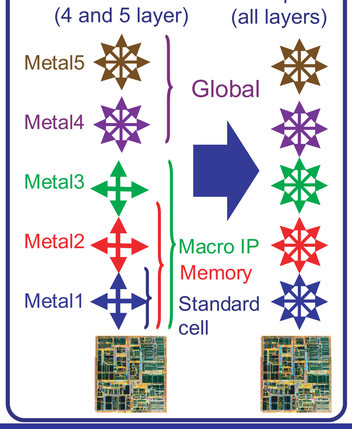


$\sqrt{2}\approx 1.41$

The total number of the interconnects, I_{total}, is unchanged

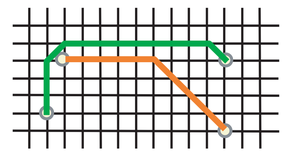
5. Assumption

1: layers
- real (4 and 5 layer)
- Assumption (all layers)

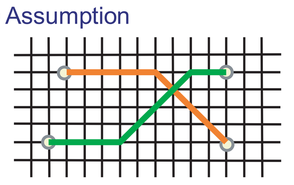


2: A gate is connected by the shortest distance.

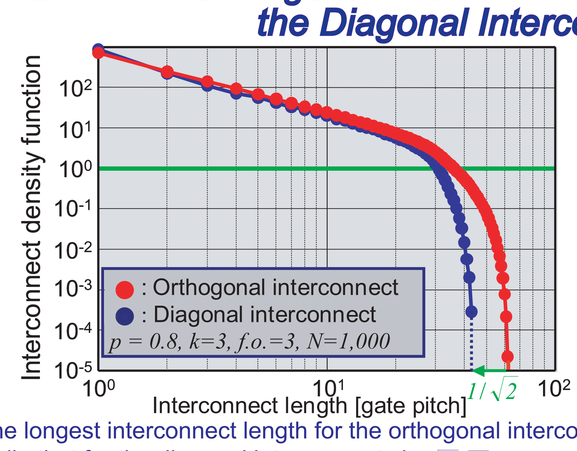
- real



- Assumption

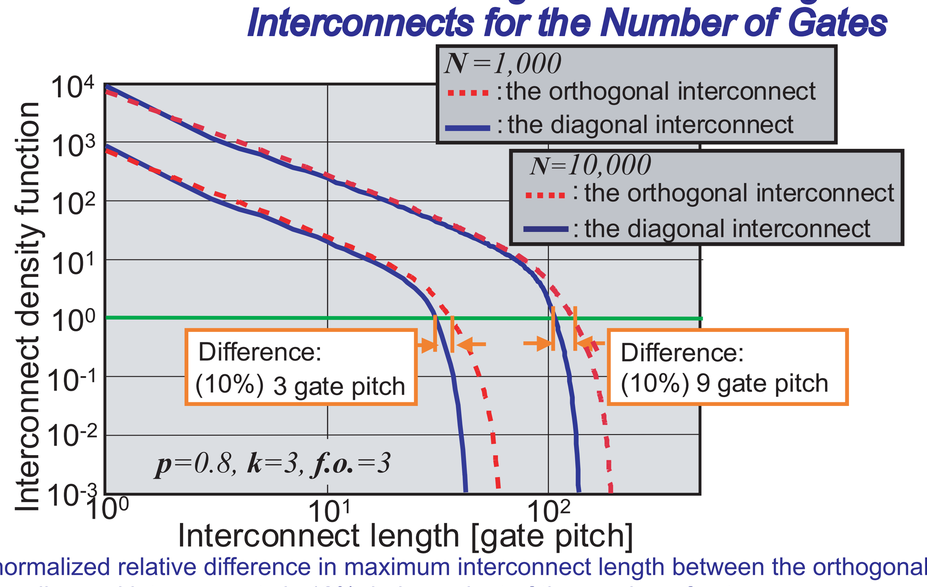


6. ILD of the Orthogonal and the Diagonal Interconnects



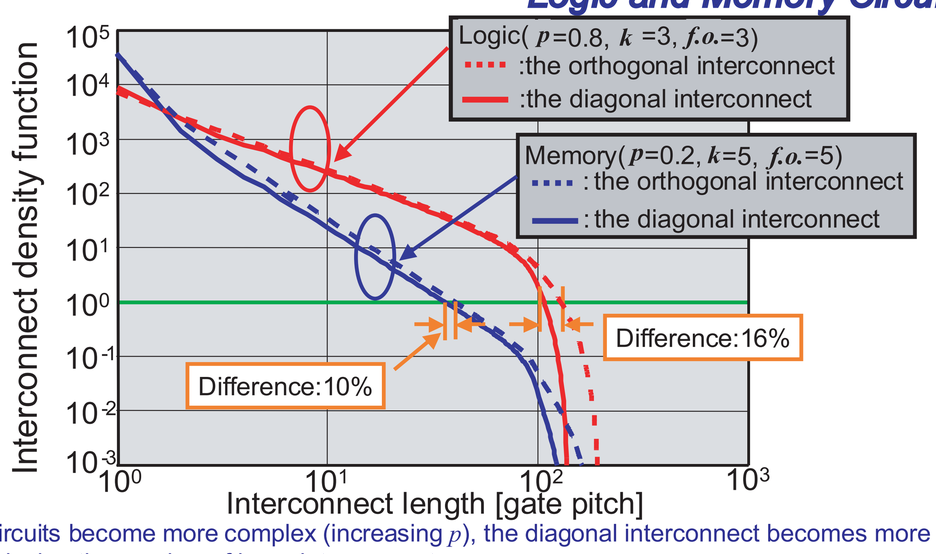
The longest interconnect length for the orthogonal interconnects is $2\sqrt{N}$, while that for the diagonal interconnects is $\sqrt{2}\sqrt{N}$.

7. ILD difference between the Orthogonal and the Diagonal Interconnects for the Number of Gates



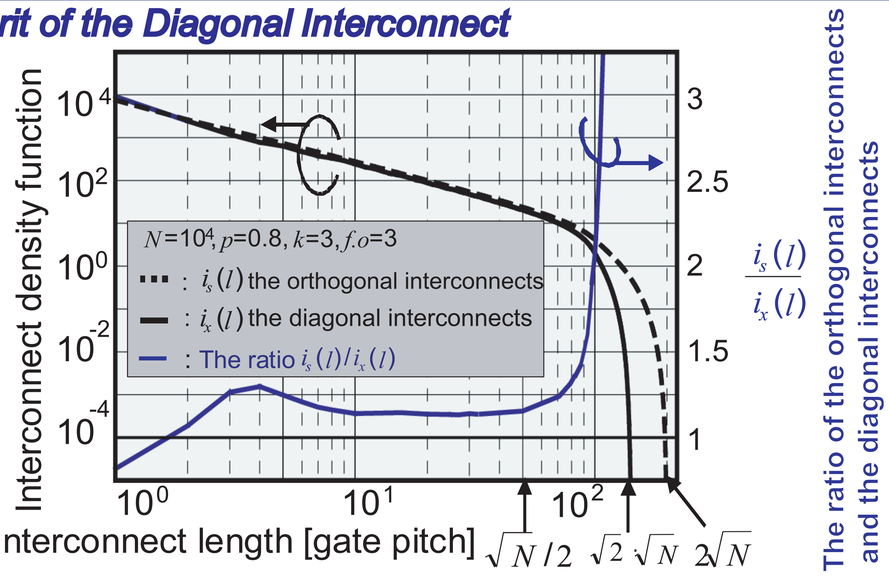
The normalized relative difference in maximum interconnect length between the orthogonal and the diagonal interconnects is 10%, independent of the number of gates.

8. ILD of the Orthogonal and the Diagonal Interconnects for Logic and Memory Circuits



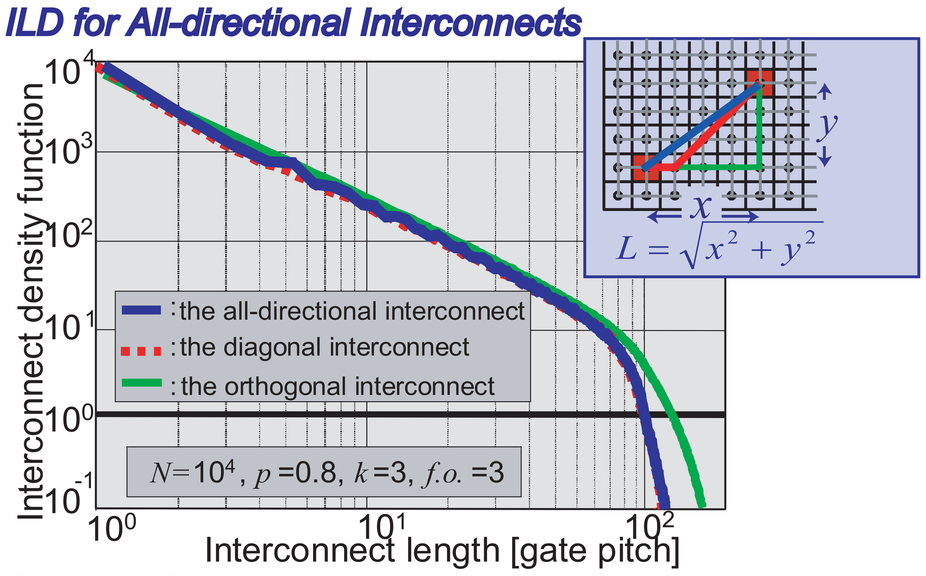
As circuits become more complex (increasing p), the diagonal interconnect becomes more effective in reducing the number of large interconnects.

9. Merit of the Diagonal Interconnect



The Diagonal interconnect reduces the number of long interconnects.

10. ILD for All-directional Interconnects



The difference of ILD between the diagonal and all-directional interconnects is very little.

11. Performance

Power Consumption and *Chip Area*

The orthogonal interconnects

l_{total} reduces 17%

Power Consumption and *Chip Area reduces 17%*

The diagonal interconnects

l_{total} is total length of interconnects

$$P=a\frac{1}{2}V_{dd}^2 f_c C_{unit} l_{total} \qquad A_C=p_m l_{total}$$

Clock Frequency

The orthogonal interconnects

l_{ave} reduces 18%

Clock frequency reduces 18%

The diagonal interconnects

l_{ave} is average interconnects length

$$T_g=R_{gout} f.o.(0.86c_{int}l_{avg}+0.86C_{gin}) + r_{int}l_{avg}(0.37c_{int}l_{avg}+0.86C_{gin})$$

H. B. Bakoglu, Circuits, Interconnections, and Packaging for VLSI. Reading, MA: Addison-Wesley, 1990.

12.Summary

1. As circuits become more complex (increasing p), the diagonal interconnect becomes more effective in reducing the number and length of interconnects.
2. Using the X Architecture instead of the conventional orthogonal interconnects, both the interconnection area and the power consumption of interconnects decrease by 17% and the clock frequency increase by 18%.
3. The difference of ILD between the diagonal and all-directional interconnects is very little. The X Architecture is sufficient to reduce the number of long interconnects.