ULSI Interconnect Length Distribution

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Background

Purpose

Interconnects Length Distribution (ILD)

Estinate of power consumption, clock frequency and chip size

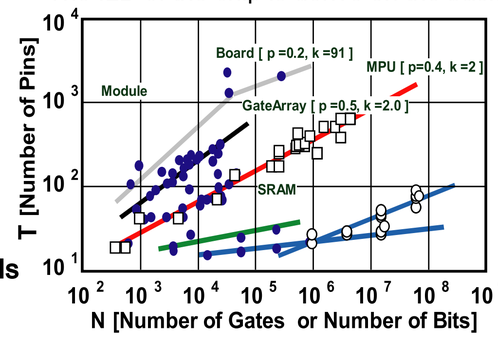
- Evaluation of a chip
- Optimization of interconnect layout

Subject

1. Derivation of Interconnect Length Distribution in Syatem LSIs
2. Paeameterextraction
3. Derivation of Interconnect Length Distribution in X Architecture LSIs
4. Extacting the ILD from netlist
5. New Analytical ILD Expression Considering Core Utilization

Rent's rule

The ILD of the chip is derive on the basis the empirical Rent's rule



Rent's rule : $T=kN^p$

- Pin T:pin of chip
- # of gates N:# oflogic block
- Rent's constant k :average # of ports of gates
- Rent's constant p :the complexity of circuits

Analytical Expression of ILD

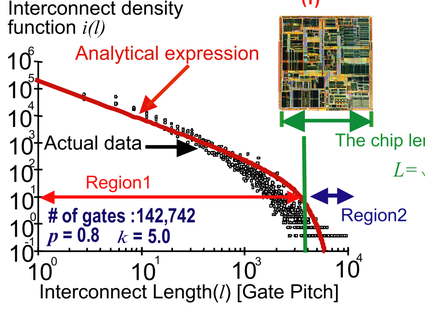
$i(l)$:# of interconnects
k&p:Rent's constants
$f.o.$:average fanout
N:# of gates

Region1: $1 \le l < \sqrt{N}$

$$i(l) = \frac{\alpha k}{2}\Gamma\left(\frac{l^3}{3} - \sqrt{2}\,Nl^2 + 2Nl\right)l^{2p-4} \quad (1)$$

Region2: $\sqrt{N} \le l < \sqrt{N}$

$$i(l) = \frac{\alpha k}{6}\Gamma\left(2\sqrt{N} - l\right)^3 l^{2p-4} \quad (2)$$



The chip length of one side is $\sqrt{N}$

$L = \sqrt{N} = 377$

$$\Gamma = \frac{2N(1-N^{p-1})}{-N^p\left(\frac{1+2p-2^{2p-1}}{p(2p-1)(p-1)(2p-3)} - \frac{1}{6p}\right) - \frac{2\sqrt{N}}{2p-1} - \frac{N}{p-1}}$$

$$\alpha = \frac{f.o.}{f.o.+1}$$

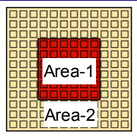
- Analytical expression shows the relation interconnect length and the number of interconnects

J.A.Davis,V.K.De,and J.D. Mindl:IEEE Trans. Electron Devices.45(1998),580-589

1.System LSI

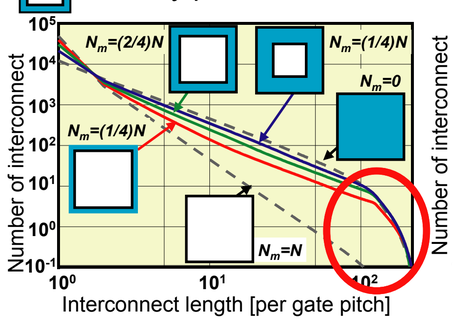
Dual function chip

Center model

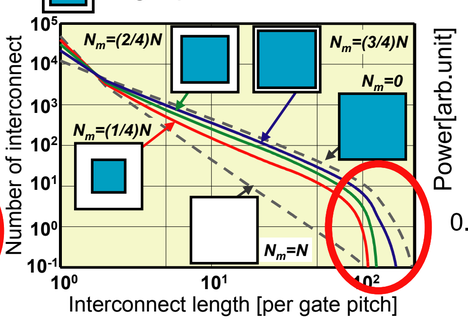


# of gates (N) : 16,384(gates)
: logic(p=0.8, k=3, $f.o.$=3)
: memory(p=0.2, k=5, $f.o.$=2)

:memory placed at center

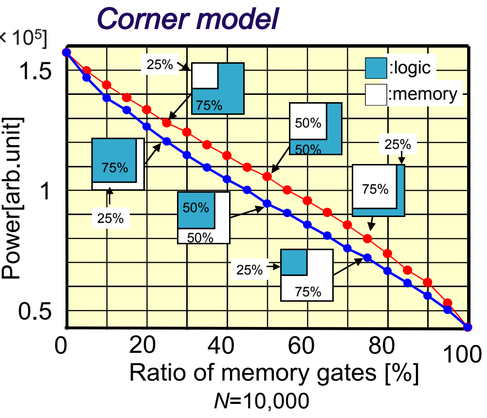


:logic placed at center

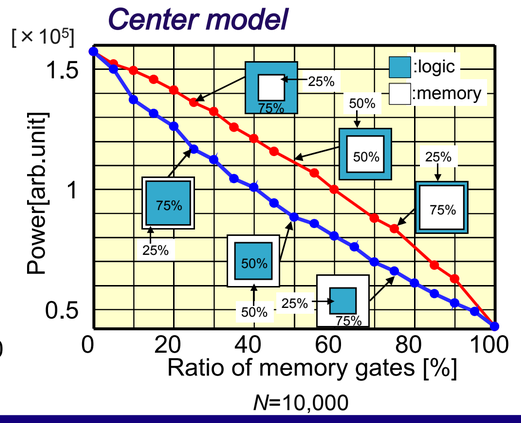


Power consumption

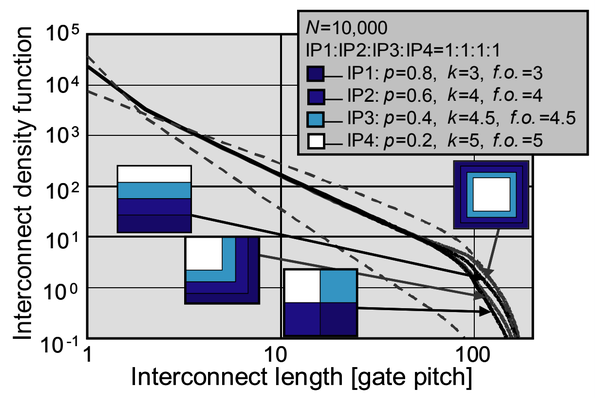
Corner model



Center model



Plural function chip

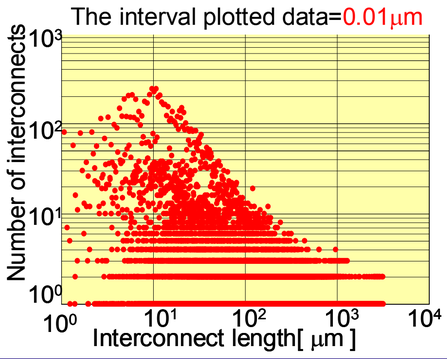


2.Parameter Extraction

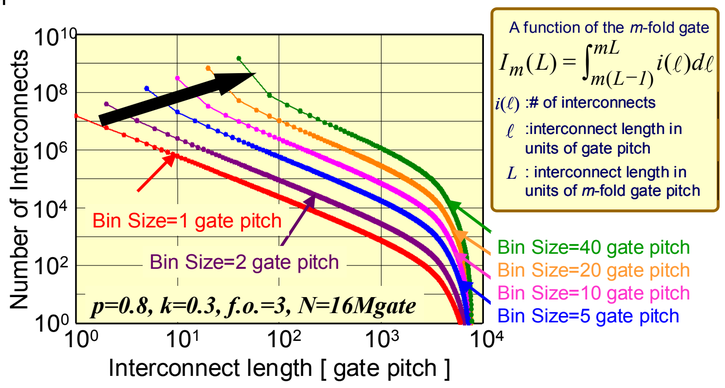
Row ILD data

Synopsys Apollo P&R summary of macro cell of 0.13mm commercially available chip

The interval plotted data=0.01μm



Simulation result

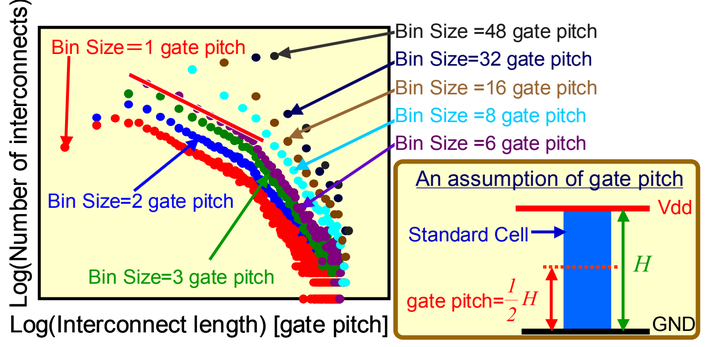


A function of the m-fold gate

$$I_m(L) = \int_{m(L-1)}^{mL} i(\ell)d\ell$$

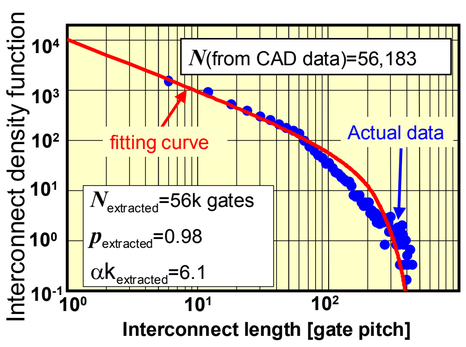
$i(\ell)$:# of interconnects
ℓ :interconnect length in units of gate pitch
L : interconnect length in units of m-fold gate pitch

ILD from wiring data



An assumption of gate pitch

Result

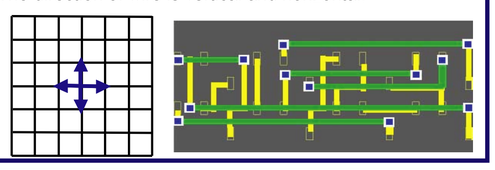


3.X Architecture

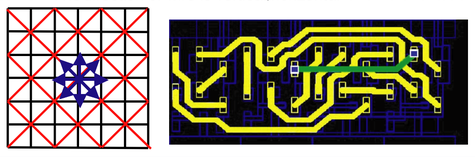
X Architecture

Reduce
# of via
Interconnect length

Standard :The direction of wire is vertical and horizontal.

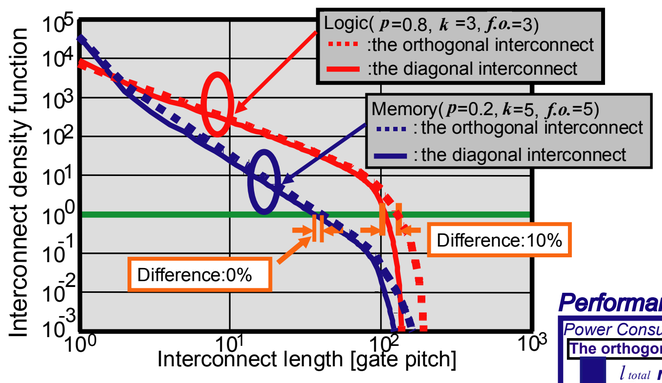


X Architecture :The direction of wire is vertical,horizontal and 45°orientation.



X initiative : http://www.xinitiative.org/wt/home_flash.php

ILD of the Orthogonal and the Diagonal Interconnects for Logic and Memory Circuits



As circuits become more complex (increasing p), the diagonal interconnect becomes more effective in reducing the number of large interconnects.

Orthogonal interconnect
$L = x + y$

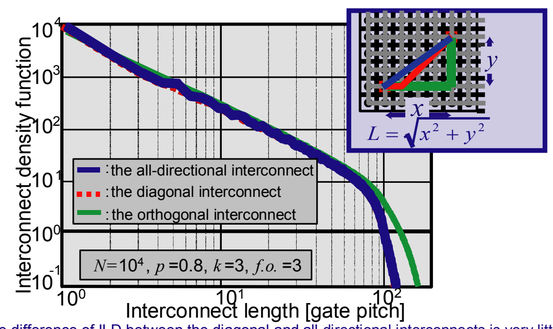
Diagonal interconnect
(X Architecture)
Using computer simulation

$L = (x-y) + y\sqrt{2}$ $(x \ge y)$

$L = (y-x) + x\sqrt{2}$ $(y > x)$

The total number of the interconnects, I_{total}, is unchanged

ILD for All-directional Interconnects



The difference of ILD between the diagonal and all-directional interconnects is very little.

Performance

Power Consumption and *Chip Area*

The orthogonal interconnects
l_{total} **reduces 17%**
Power Consumption and Chip Area reduces 17%
The diagonal interconnects

l_{total} is total length of interconnects

$$P = a\frac{1}{2}V_{dd}^2 f_c C_{unit} l_{total} \qquad A_C = p_m l_{total}$$

Clock Frequency

The orthogonal interconnects
l_{ave} **reduces 18%**
Clock frequency reduces 18%
The diagonal interconnects

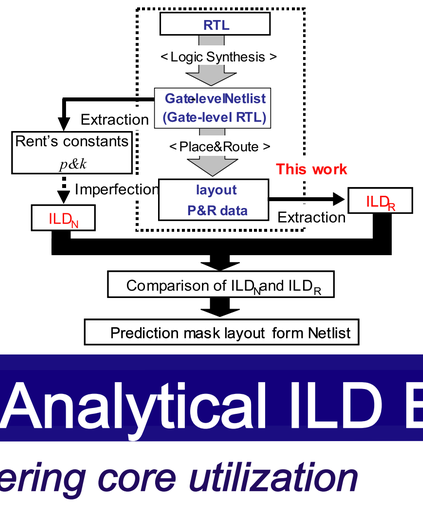
l_{ave} is average interconnects length

$$T_g = R_{gout} f.o.(0.86c_{int}l_{avg} + 0.86C_{gin}) + r_{int}l_{avg}(0.37c_{int}l_{avg} + 0.86C_{gin})$$

H. B. Bakoglu, Circuits, Interconnections, and Packaging for VLSI. Reading, MA: Addison-Wesley, 1990.

4.Extracting the ILD from Netlist

Purpose of this work



Extracting the ILD paraeters

ILD parameters: N, k, f.o., p

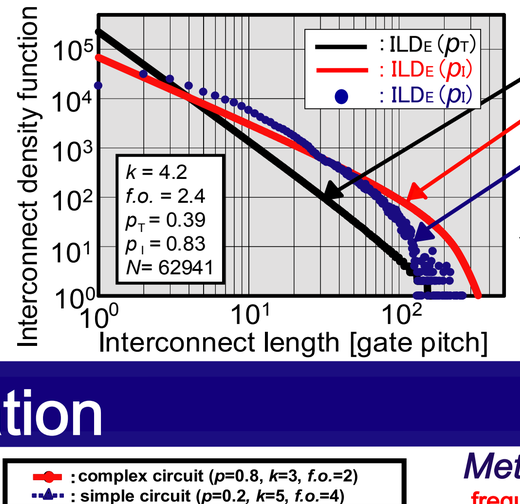
Netlist

The followingparameters are listed: N, k, f.o.

We propos two methods of Rent's constant p extraction.

1. *Rent's rule :* $T = kN^{p_T}$
2. *Total number of interconnect I:* $I = \frac{f.o.}{f.o.+1}k(N - N^{p_I})$

Result



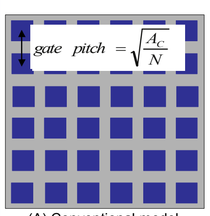
Average interconnect length

L_E (p_T)= 14.9 μm
L_E (p_I)= 81.9 μm
L_R = 64.2 μm

ILDE is the amalytical ILD expression.
– ILDR is the ILD of the layout data.–

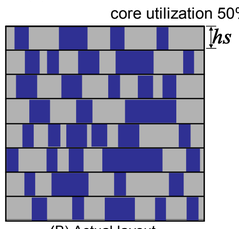
5.New Analytical ILD Expression Considering Core Utilization

ILD considering core utilization



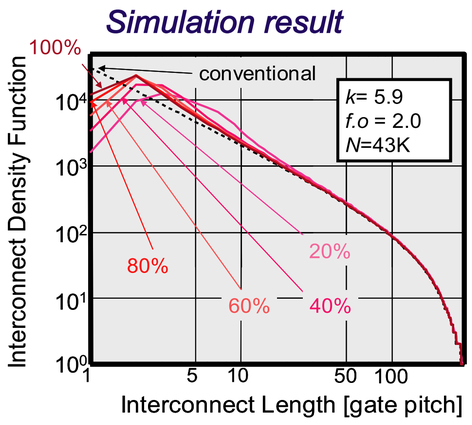
(A) Conventional model

core utilization 50%

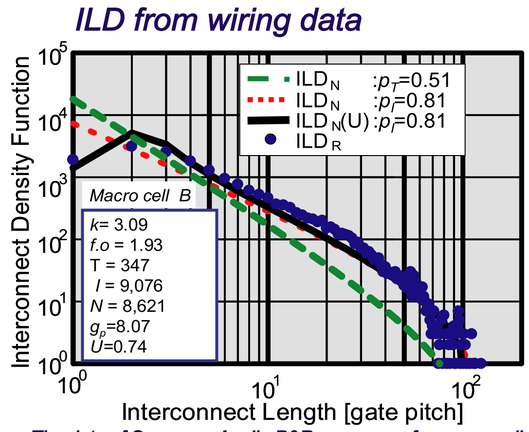


(B) Actual layout

Simulation result



ILD from wiring data

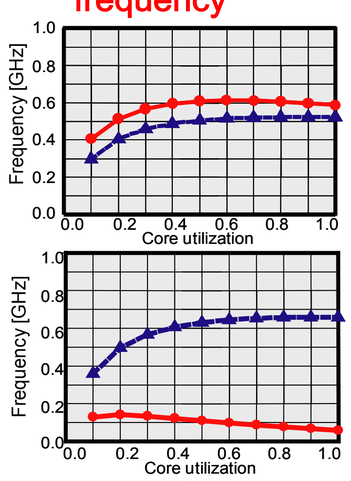


The data of Synopsys Apollo P&R summary of a macro cell of a commercially available 0.18mm chip.

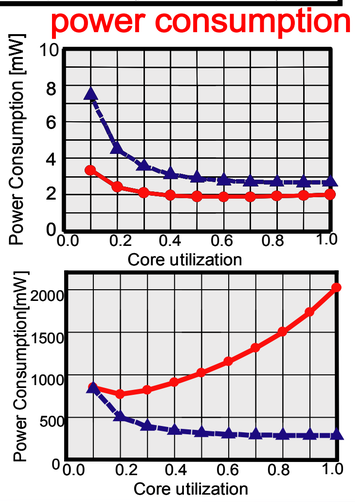
Performance

: complex circuit (p=0.8, k=3, $f.o.$=2)
: simple circuit (p=0.2, k=5, $f.o.$=4)

frequency

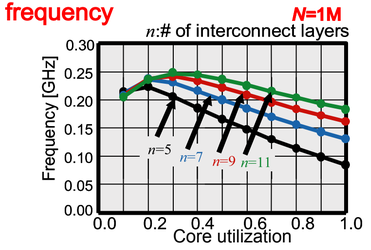


power consumption



Metal layers

frequency N=1M



power consumption N=1M