Background

Purpose
Interconnects Length Distribution (ILD)
- Estimate of power consumption, clock frequency and chip size
- Optimization of interconnect layout

Subject
1. Derivation of Interconnect Length Distribution in System LSIs
2. Parameter extraction
3. Derivation of Interconnect Length Distribution in X Architecture LSIs
4. Extracting the ILD from netlist
5. New Analytical ILD Expression Considering Core Utilization

1. System LSI
Dual function chip
Center model
- Logic placed at center
- Memory placed at center

2. Parameter Extraction
Row ILD data
- Synopsys Apollo P&R summary of macro cell of 0.13m commercially available chip
- The interval plotted data = 10
- Simulation result
- Power consumption

3. X Architecture
X Architecture
- Standard: The direction of wire is vertical and horizontal
- Reduce # of via
- X Architecture expresses the interconnect density and difference

4. Extracting the ILD from Netlist
Purpose of this work
- ILD parameters: N, k, f_o, p
- Netlist
- We propose two methods of Rent’s constant extraction
  1. Rent’s rule: T = \( p^N \)
  2. Total number of interconnect: \( I = \frac{(k-1)}{f_o \cdot p} \)

5. New Analytical ILD Expression Considering Core Utilization
ILD considering core utilization
- Simulation result
- ILD from wiring data
- Performance
- Power consumption
- Metal layers
- Frequency