Wire Length Distribution Model Considering Core Utilization for SoC

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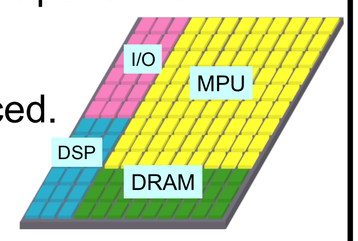
1. Background

In recent years, a lot of system LSIs are designed.

LSI design based on IP (Intellectual Properties)

Development of circuit as a component of a SoC (System on a Chip).

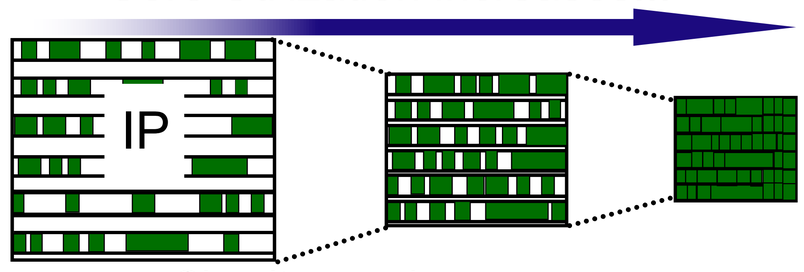
1. Manufacturing cost is reduced.
2. Design time is reduced.



➡ Deciding area allocation of IP is important.

How to change circuit area of IP...

Core Utilization increases...



Circuit area decreases.

→ RC interconnect delay changes.

Circuit area has large impact on performance[2]

In the recent technology, interconnect delay determines the circuit performance.

Trade-Off

Core Utilization	low	high
Interconnect Length (Resistance/Capacitance)	long (large)	short (small)
Interconnect Density (Capacitance)	low (small)	high (large)

We use Wire Length Distribution model to estimate resistance and capacitance.

2. Wire Length Distribution Model (WLD)

Analytical Expression of WLD[1]

$i(l)$:# of interconnects
k&p:Rent's constants
$f.o.$:average fanout
N:# of gates

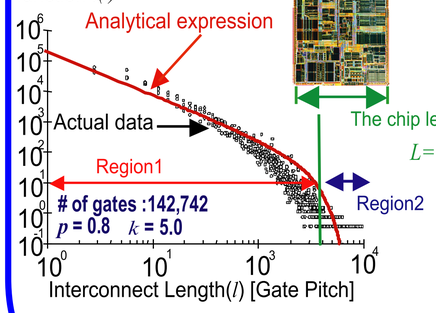
Region1: $1 \le l < \sqrt{N}$

$$i(l) = \frac{\alpha k}{2}\Gamma\left(\frac{l^3}{3} - \sqrt{2}Nl^2 + 2Nl\right) l^{2p-4} \quad (1)$$

Region2: $\sqrt{N} \le l < \sqrt{N}$

$$i(l) = \frac{\alpha k}{6}\Gamma\left(2\sqrt{N} - l\right)^3 l^{2p-4} \quad (2)$$

Interconnect density function $i(l)$



The chip length of one side is $\sqrt{N}$

$L = \sqrt{N} = 377$

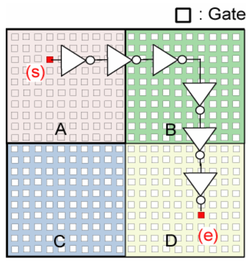
$$\Gamma = \frac{2N(1-N^{p-1})}{-N^p\left(\frac{1+2p-2^{2p-1}}{p(2p-1)(p-1)(2p-3)} - \frac{1}{6p}\right) - \frac{2\sqrt{N}}{2p-1} + \frac{N}{p-1}}$$

$$\alpha = \frac{f.o.}{f.o.+1}$$

- Analytical expression shows the relation interconnect length and the number of interconnects

J.A.Davis,V.K.De,and J.D. Mindl:IEEE Trans. Electron Devices.45(1998).580-589

WLD for SoC



We must consider

inter-macro wires
+
each core utilization of macro blocks

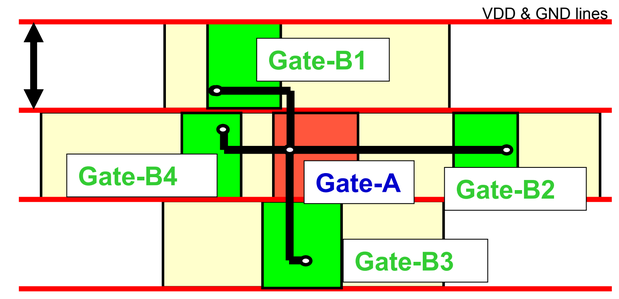
We propose a new model considering both effect.

Assumption

- Global layer is used to connect macro blocks
- Gate size of repeaters is optimized*.

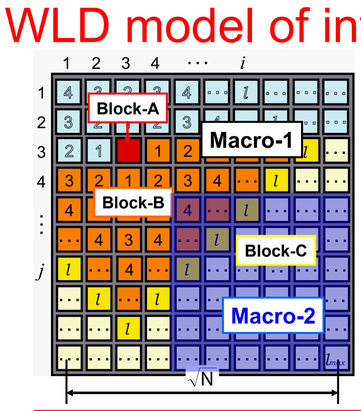
* H. B. Bakoglu et. al., "Circuits, Interconnections, and Packaging for VLSI", (1990)

WLD model of each macro blocks [2]

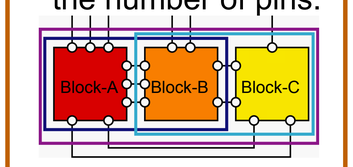


Gate is arranged in random size and position.

WLD model of inter-macro wires [3]



Algorithm to count the number of pins.

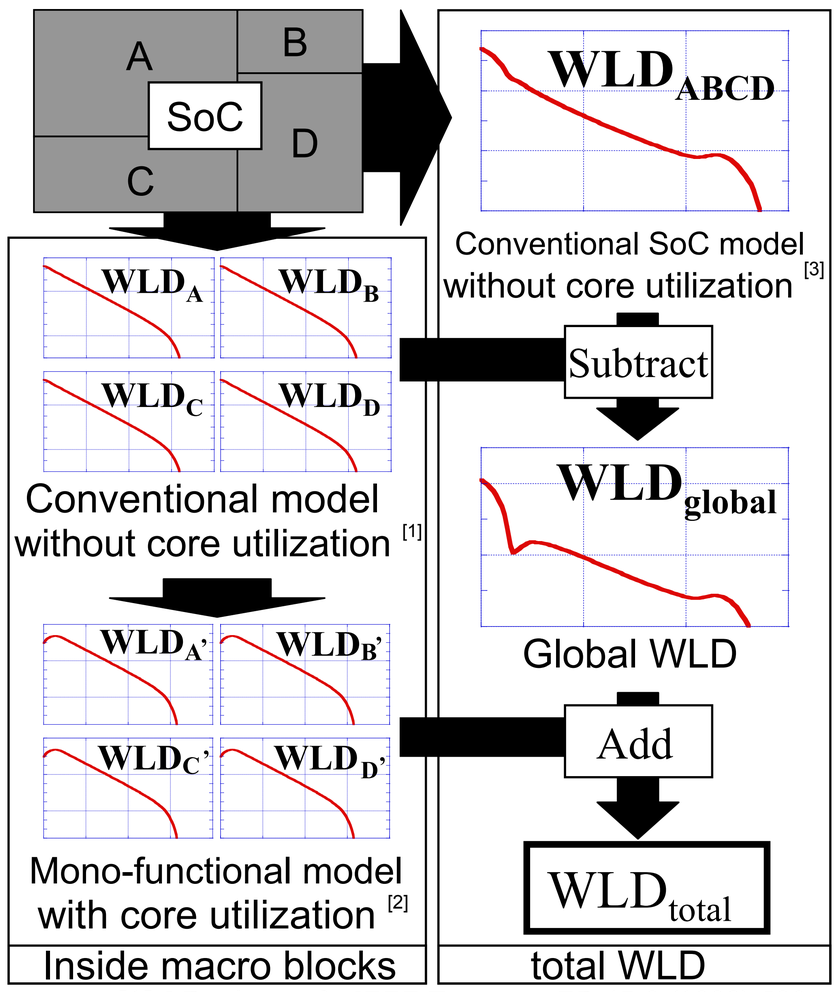


$$T_{A\,to\,C} = T_{AB} - T_B + T_{BC} - T_{ABC}$$

T_{AB} = Number of pins going out from Blocks (A + B)
T_B = Number of pins of Block - B
T_{BC} = Number of pins going out from Blocks (B + C)
T_{ABC} = Number of pins going out from Blocks (A + B + C)

Step 1
Block-C has the distance ℓ from Block-A.
Block-B has the distance less than ℓ.
Step 2
Count the number of I/O pins connecting Block-A to Block-C (T_{AtoC}).
Step 3
Apply Step1,2 to all the gates of a circuit

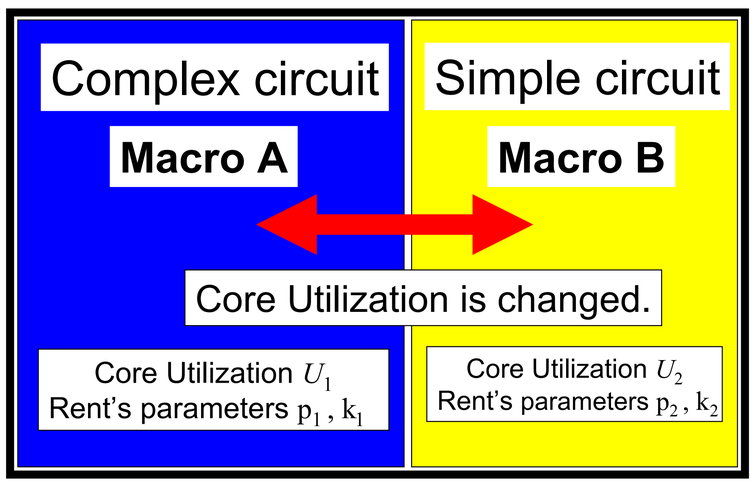
The derivation flow of proposed WLD model



[1] J.Davis *et. al., IEEE Trans. on ED* **45-3** (1998) 580
[2] H.Nakashima *et.al., Proc. IEEE DATE* **2**(2004) 1210
[3] T.Kyogoku *et.,al., Proc. SASIMI* (2005) 176

3. Results

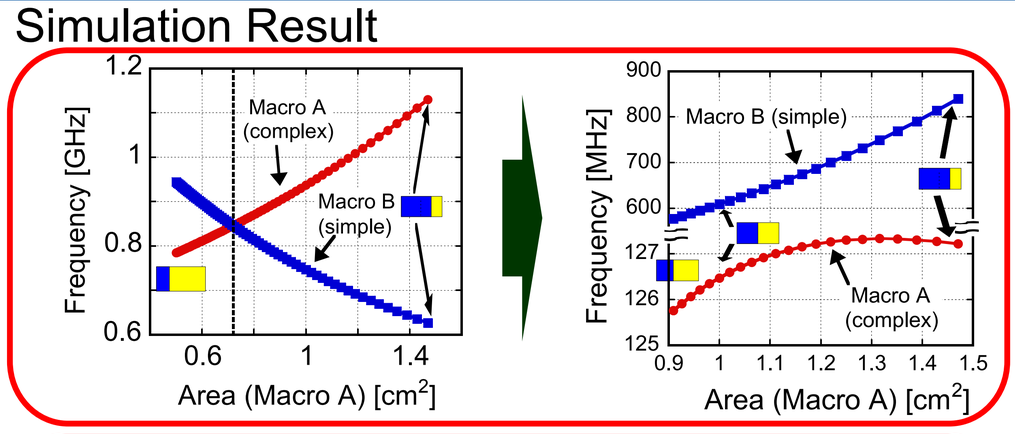
Chip model

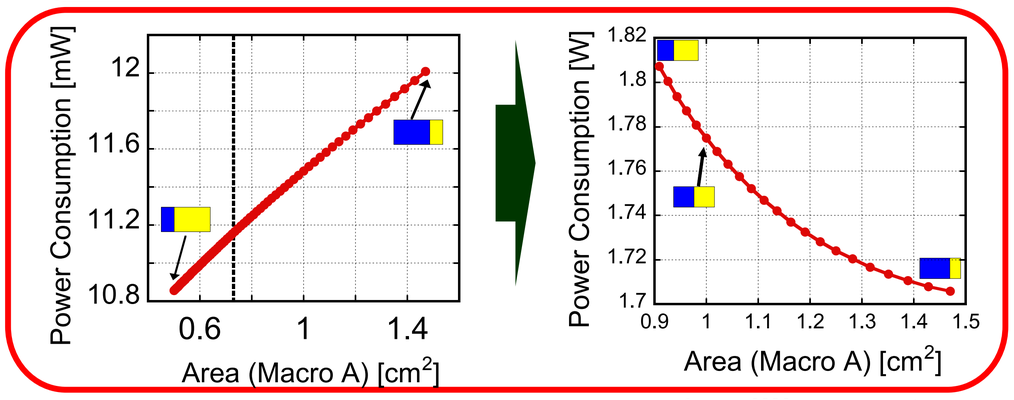


- These macros have the same number of gate.
- Chip has 2 macro blocks.
- Total chip area is fixed.
- Area of complex circuit is changed.
- Area of Macro B is decided automatically.

chip size = $2cm^2$
$p_1 = 0.8$, $p_2 = 0.2$
$k_1 = 3$, $k_2 = 6$
$0 < U_1, U_2 \leqq 1$

Simulation Result





10, 000 gate　　1 million gate

The number of gates increases,

➡ The operating frequency is limited by that of Macro A.

➡ Operating frequency has less effect.

The number of gates increases,

➡ Complex circuit area (Macro A) must be expanded to reduce total power consumption.

➡ Area of macro block must be large as long as operating frequency is not violated.

4. Conclusion

Area allocation of macro blocks inside SoC is important.

>>> The area of circuit which have large number of gate must be expanded to reduce power consumption.

Future work --- To consider the influence of VIA and to simulate real cell placement.