Development of Differential Transmission Line Interconnect IP for High-Speed Global Interconnect

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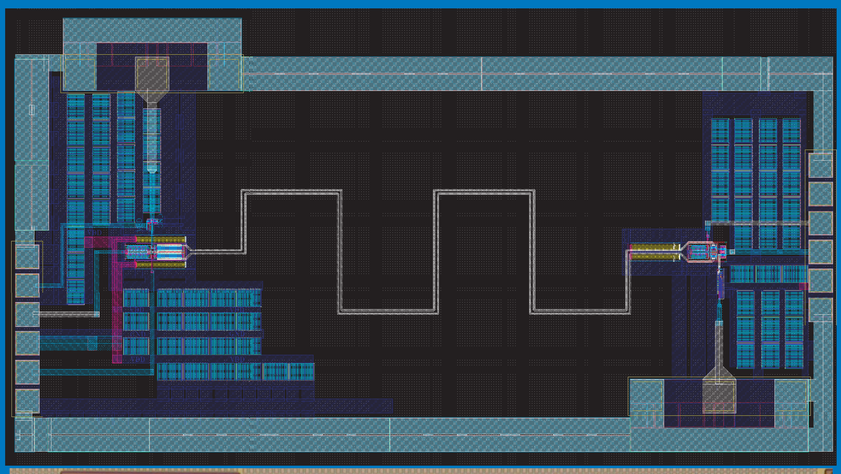
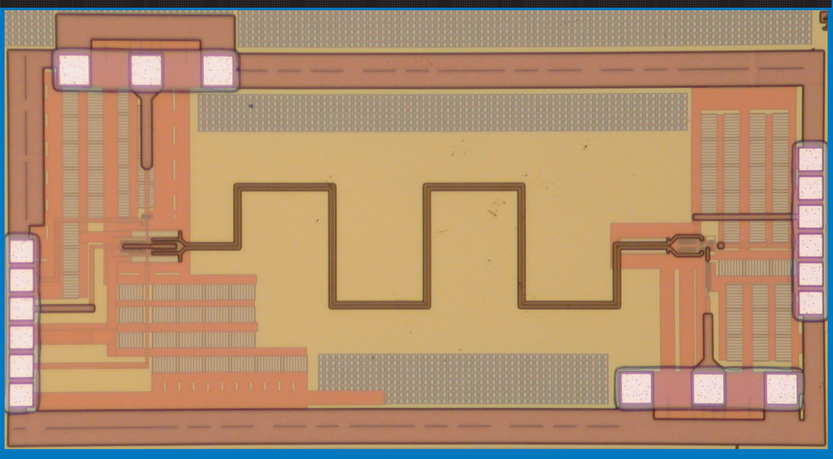




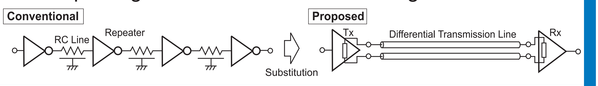
Background

Issues for Si LSI:
Delay and Power Dissipation in Long Global Interconnects

Transmission Line Interconnect:
Faster signaling than a conventional RC interconnect

Aim

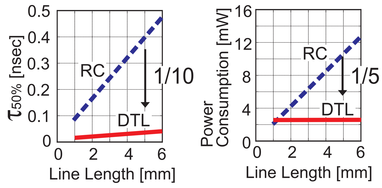
Implementation of high-speed transmission line interconnect IP to replace global RC interconnect in a digital LSI



Impact

Numerical Results at 45nm Technology Node

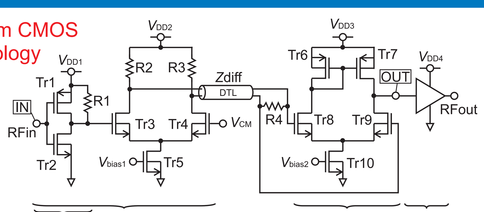
H. Ito, *et al.* IEEE IEDM, pp. 677-680, Dec. 2004.



The circuit with DTL interconnects can save 30 % power.
The operating frequency can be improved from 15 GHz to 40 GHz by using DTL interconnect.

Schematic & Line Structure

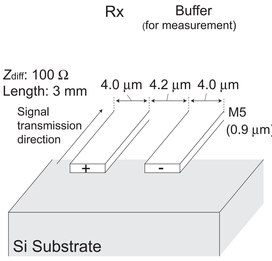
0.18 μm CMOS Technology



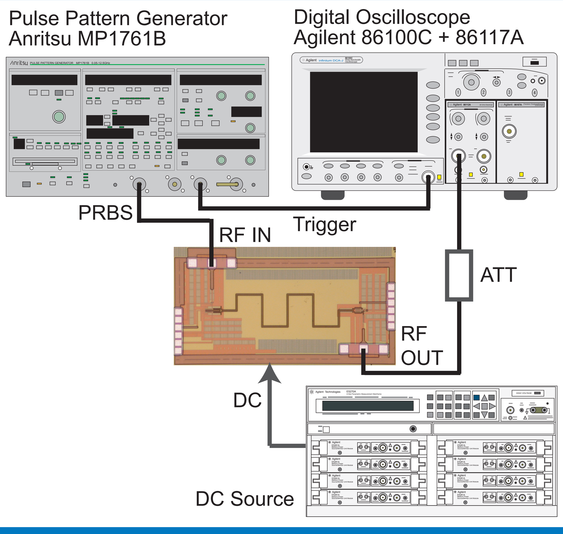
Component	Tr1	Tr2
W / L	10 μm / 0.2 μm	10 μm / 0.2 μm
Component	Tr3, Tr4	Tr5
W / L	310 μm / 0.2 μm	300 μm / 0.4 μm
Component	Tr6, Tr7	Tr8
W / L	20 μm / 0.2 μm	20 μm / 0.2 μm
Component	Tr10	
W / L	20 μm / 0.4 μm	

Component	R1	R2	R3	R4
Value	250 Ω	50 Ω	50 Ω	100 Ω

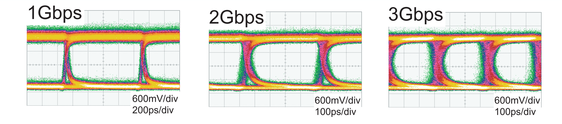
Source	V_{DD1}	V_{DD2-4}	V_{bias1}	V_{CM}	V_{bias2}
Value	1.00 V	1.80 V	0.55 V	1.32 V	0.55 V

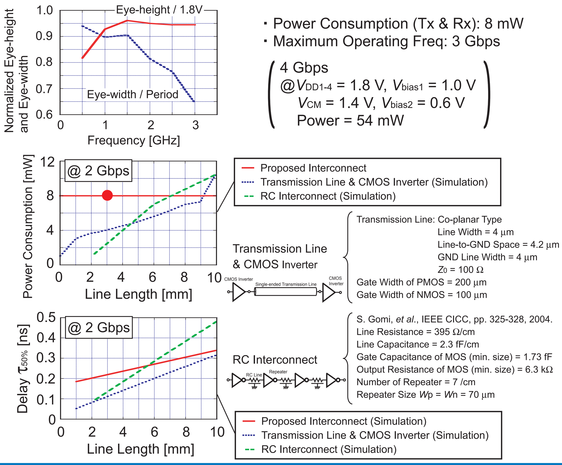


Measurement System



Measurement Results





Summary

- Purpose of this work is implementation of high-speed transmission line interconnect IP to replace global RC interconnect in a digital LSI.
- Maximum 4 Gbps signaling can be achieved using the proposed circuit fabricated by 0.18 μm CMOS technology.
- The proposed interconnect has smaller power consumption and delay than the conventional RC interconnect over 7 mm as 2 Gbps signaling.
- The transmission line interconnect is one of the promising technology to overcome power and delay issues for long global interconnect.