4 Gbps On-Chip Interconnection using Differential Transmission Line

Hiroyuki Ito, Hideyuki Sugita, Kenichi Okada, and Kazuya Masu
Precision and Intelligence Laboratory, Tokyo Institute of Technology

Background

Issues for Si LSI:

- Delay and Power Dissipation in Long Global Interconnects

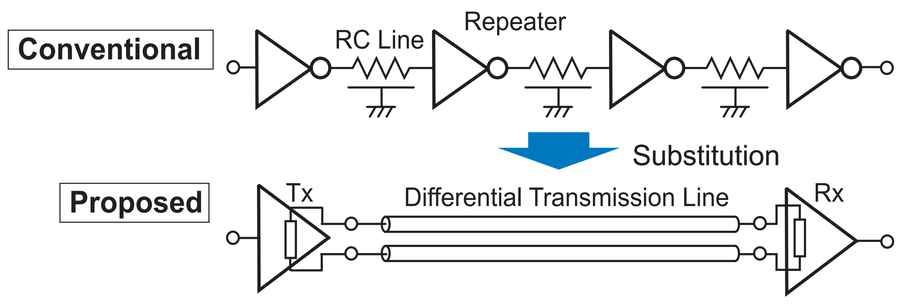
  Designed as RC lines, Divided by several reqeaters

Transmission Line Interconnect:

- - Faster signaling than a conventional RC interconnect
- (Signals can propagate at electromagnetic-wave speed.)
- - Power consumption does not depend on a line length.
- (Repeaters are not necessary for high-speed signaling.)

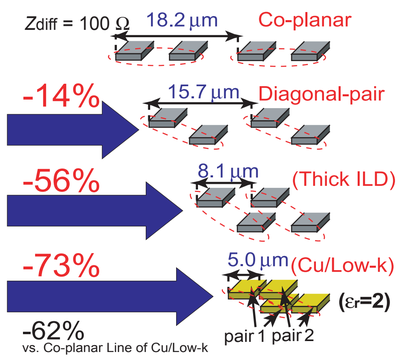
Purpose of This Work

Implementation of high-speed transmission line interconnect IP to replace global RC interconnect in a digital LSI

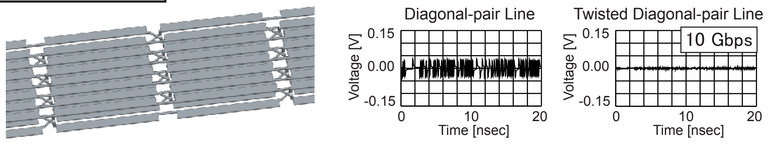


Previous Work

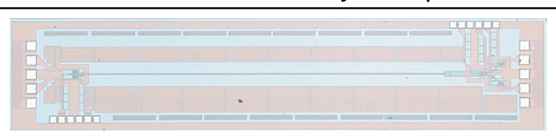
Diagonal-pair line



Twisted line



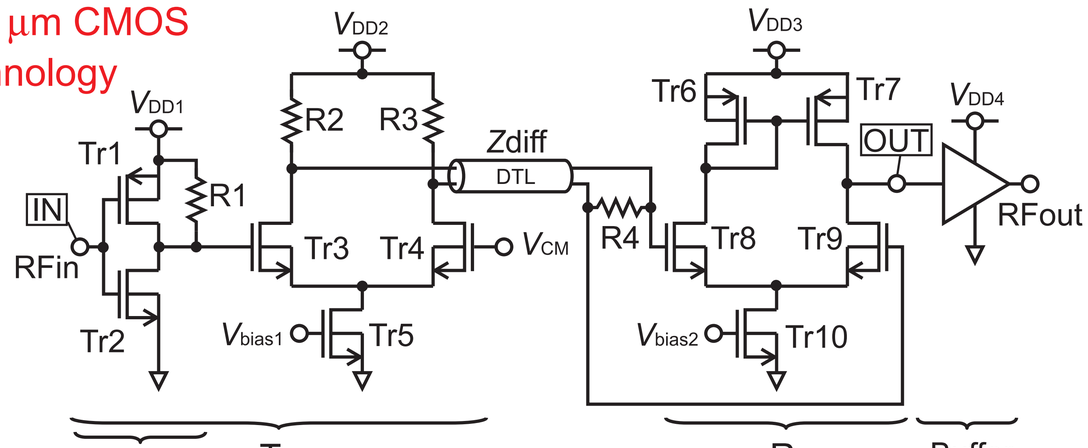
TL interconnect fabricated by 0.35 μm CMOS technology



Differential input/output

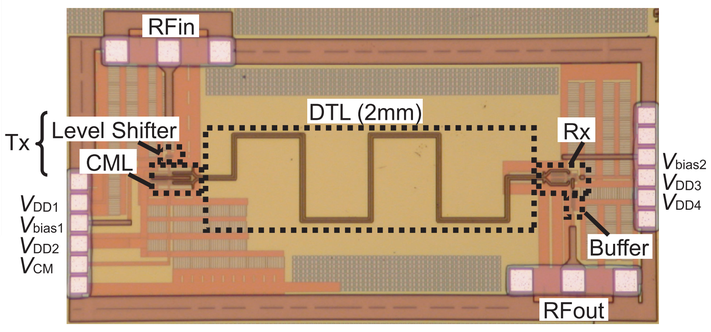
Schematic & Micrograph

0.18 μm CMOS Technology



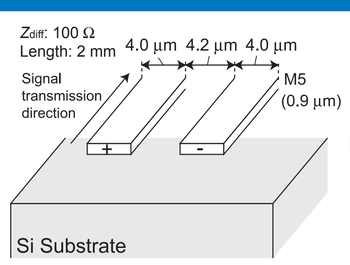
Component	Tr1	Tr2
W / *L*	10 μm / 0.2 μm	10 μm / 0.2 μm
Component	Tr3, Tr4	Tr5
W / *L*	310 μm / 0.2 μm	300 μm / 0.4 μm
Component	Tr6, Tr7	Tr8, Tr9
W / *L*	20 μm / 0.2 μm	20 μm / 0.2 μm
Component	Tr10	
W / *L*	20 μm / 0.4 μm	

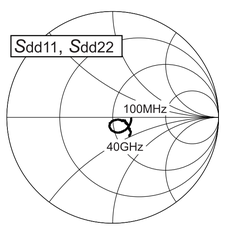
Component	R1	R2	R3	R4
Value	250 Ω	50 Ω	50 Ω	100 Ω
Source	*V*DD1-4	*V*bias1	*V*CM	*V*bias2
Value	1.80 V	1.20 V	1.40 V	0.60 V

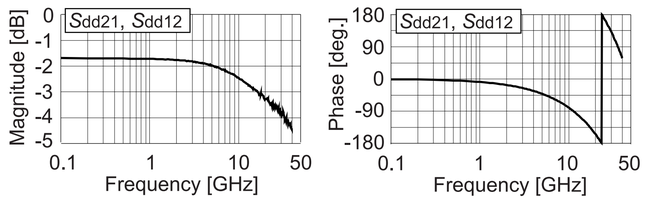


Areas of Tx and Rx are 9700 μm² and 8000 μm².

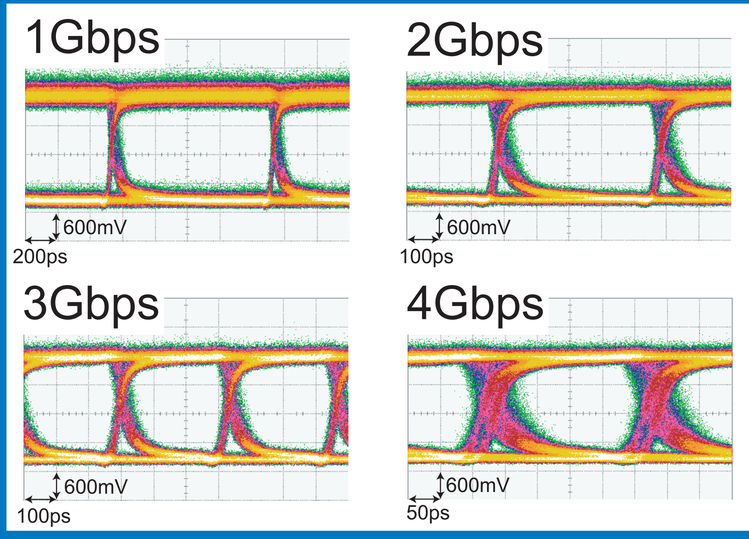
Transmission Line

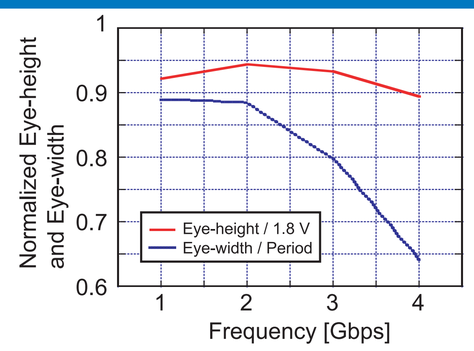






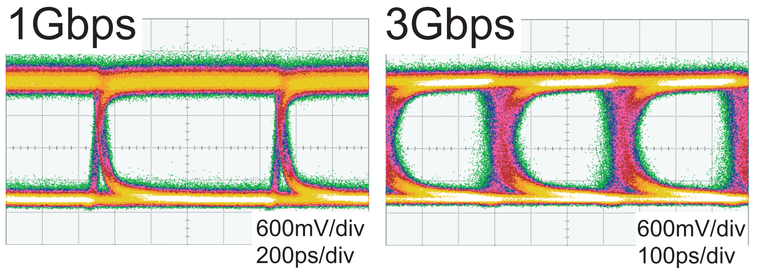
Measurement Results





- 4 Gbps signal transmission
- Consumption currents:
  - Level Shifter: 1.6 mA
  - CML of Tx: 31.7 mA
  - Rx: 2.4 mA

Low Power Mode



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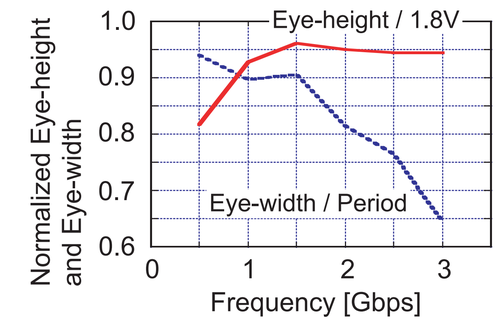
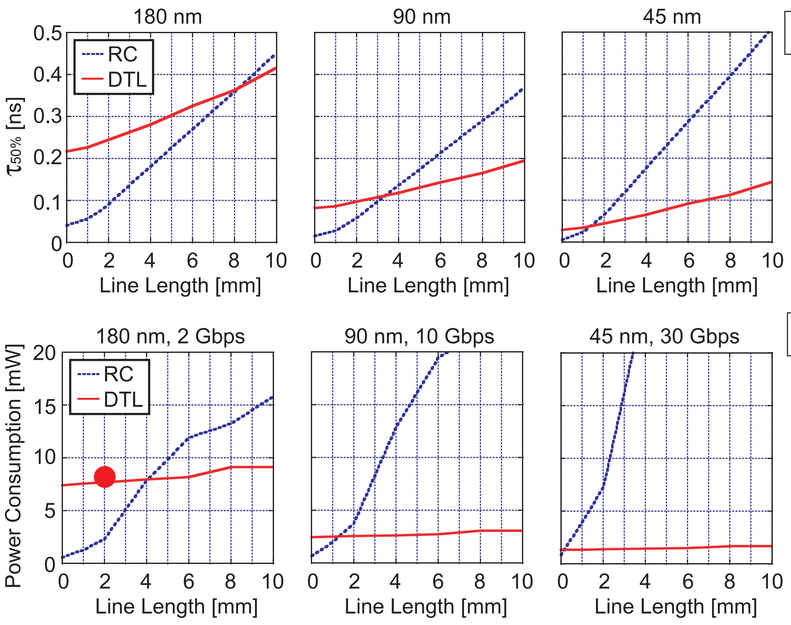


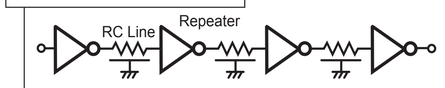
- Power Consumption (Tx & Rx): 8 mW
- Maximum Operating Freq: 3 Gbps

Impact



The proposed interconnect has the potential to achieve 3 times faster and 96 % lower power interconnect than the conventional RC interconnect at the 6mm-long line of 45 nm technology node.

RC Interconnect



Line Resistance = 37 Ω/mm
Line Capacitance = 0.20 pF/mm
(Line Self-Inductance = 0.97 nH/mm)
Number of Repeater = 1 /mm
Repeater Size *W*n = 70 μm, *W*p = 140 μm

Assumption (90nm & 45nm)

$$\tau_{50\%\text{ of DTLint}} = \tau_{50\%\text{ of Tx\&Rx}} + \tau_{50\%\text{ of DTL}}$$

$$\tau_{50\%\text{ of Tx\&Rx}} \propto \frac{1}{f_T} \qquad \tau_{50\%\text{ of DTL}} \propto \ell\sqrt{\varepsilon_r}$$

$$\tau_{50\%\text{ of RCint}} = \tau_{50\%\text{ of CMOS Inverter}} + \tau_{50\%\text{ of RC Line}}$$

$$\tau_{50\%\text{ of CMOS Inverter}} \propto \frac{1}{f_T}$$

$$\tau_{50\%\text{ of RC Line}} \propto \ell\sqrt{\frac{S\varepsilon_r}{\sigma}}$$

$$P_{\text{DTLint}} \propto \frac{V_{DD}}{\mu_n} \qquad P_{\text{RCint}} \propto \ell f (C_g + C_{\text{int}}) {V_{DD}}^2$$

Conclusion

- Maximum 4 Gbps signaling can be achieved using the proposed circuit fabricated by 0.18 μm CMOS technology.
- The proposed interconnect has smaller power consumption and delay than the conventional RC interconnect over 8 mm as 2 Gbps signaling.
- The transmission line interconnect is one of the promising technology to overcome power and delay issues for long global interconnect.