A Loss Optimization Method Using WD Product for On-Chip Differential Transmission Line Design

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Background

Miniaturization of Si CMOS process

- Cut-off frequency of the NMOS transistor is projected to become 300 GHz at 45 nm technology node in 2010.
  = Clock frequency of digital circuit will reach 15 GHz.
- RF CMOS circuits that can operate at over 10 GHz are reported.

On-chip transmission lines have been becoming increasingly important for high-speed digital and RF circuits.

Problems in transmission line design specific to Si LSI

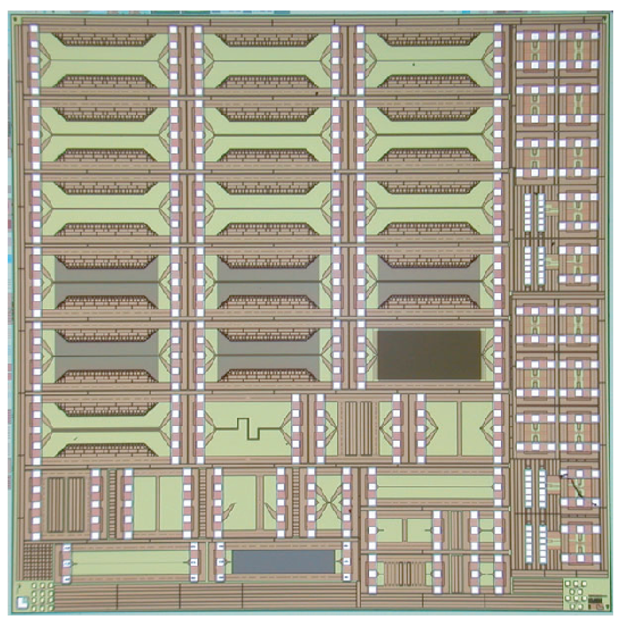
- Dielectric loss in Si substrate
- Large resistive loss due to the skin effect and the eddy current in Si substrate

Why WD product?

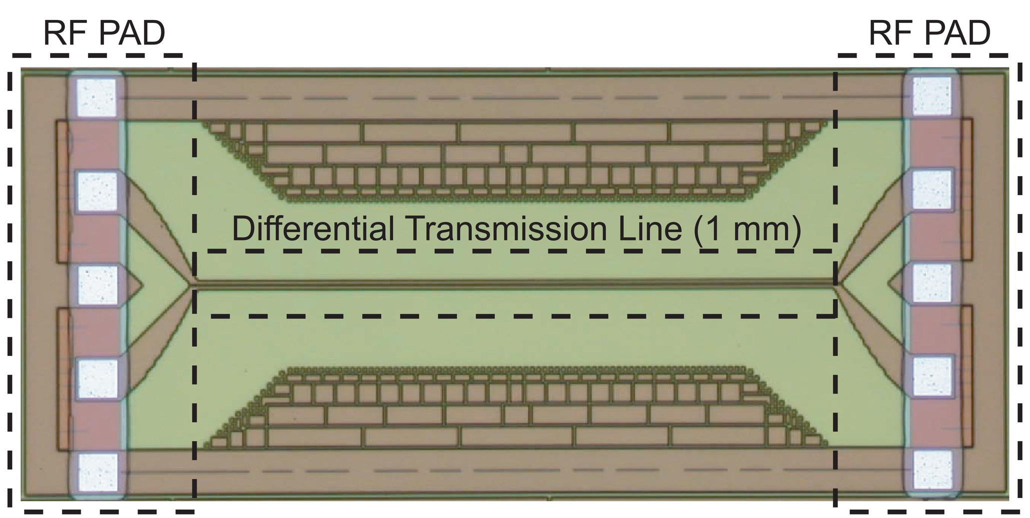
W: Line width, *D*: Distance between lines

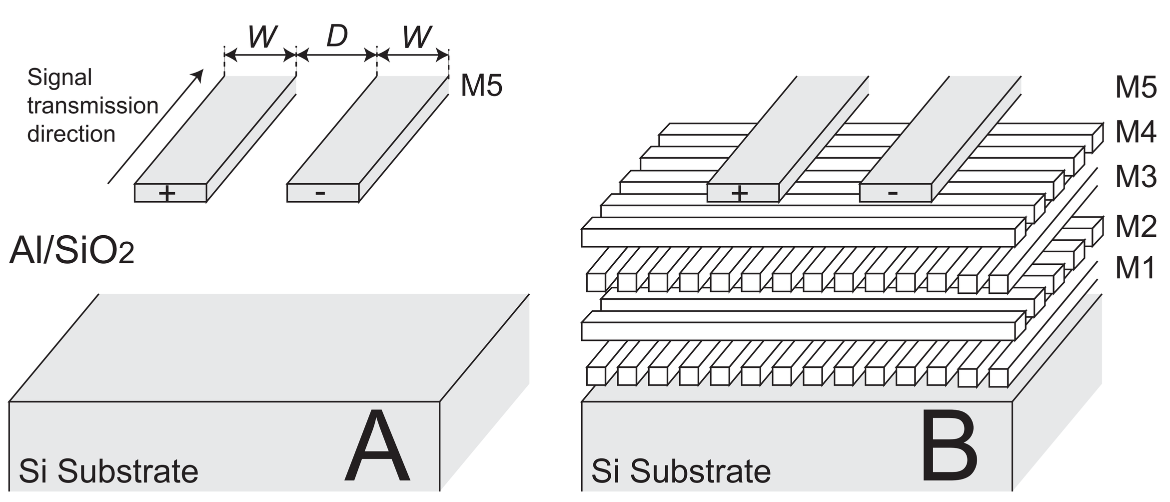
The *WD* product can give the attenuation characteristics of the transmission line.

Structures of DUTs



0.18 μm Standard Si CMOS Process



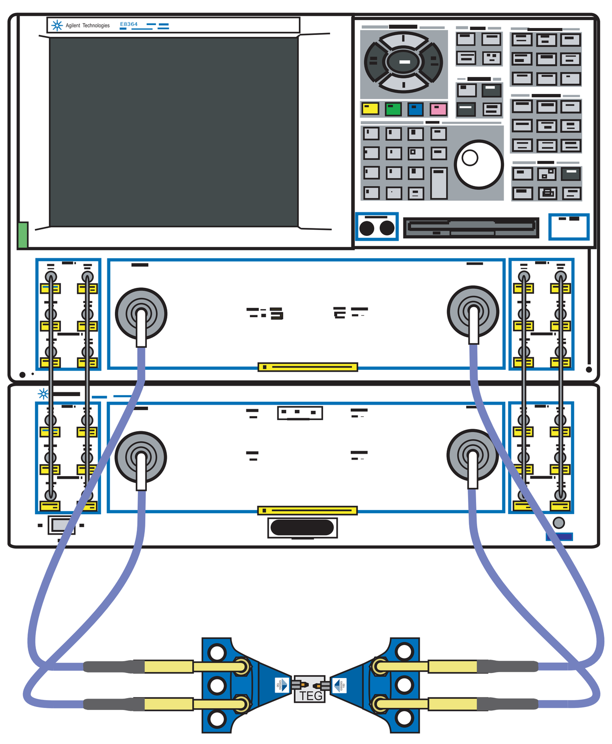


W	*D*	*WD*	Lossless Z_{diff}	Type
2.0 μm	1.8 μm	3.6	80 Ω	A
2.0 μm	2.9 μm	5.8	100 Ω	A
2.0 μm	4.3 μm	8.6	120 Ω	A
4.0 μm	2.3 μm	9.2	80 Ω	A
4.0 μm	3.7 μm	14.8	100 Ω	A
4.0 μm	5.8 μm	23.2	120 Ω	A
6.0 μm	2.6 μm	15.6	80 Ω	A
6.0 μm	4.6 μm	27.6	100 Ω	A
6.0 μm	7.4 μm	44.4	120 Ω	A
10.0 μm	11.0 μm	110.0	120 Ω	A
4.0 μm	2.3 μm	9.2	80 Ω	B
4.0 μm	3.7 μm	14.8	100 Ω	B
4.0 μm	5.8 μm	23.2	120 Ω	B
2.0 μm	2.9 μm	5.8	100 Ω	B
6.0 μm	4.6 μm	27.6	100 Ω	B

- Thicknesses of metal and dielectric layers: ≈1 μm
- A line length of the differential transmission line (DTL): 1 mm

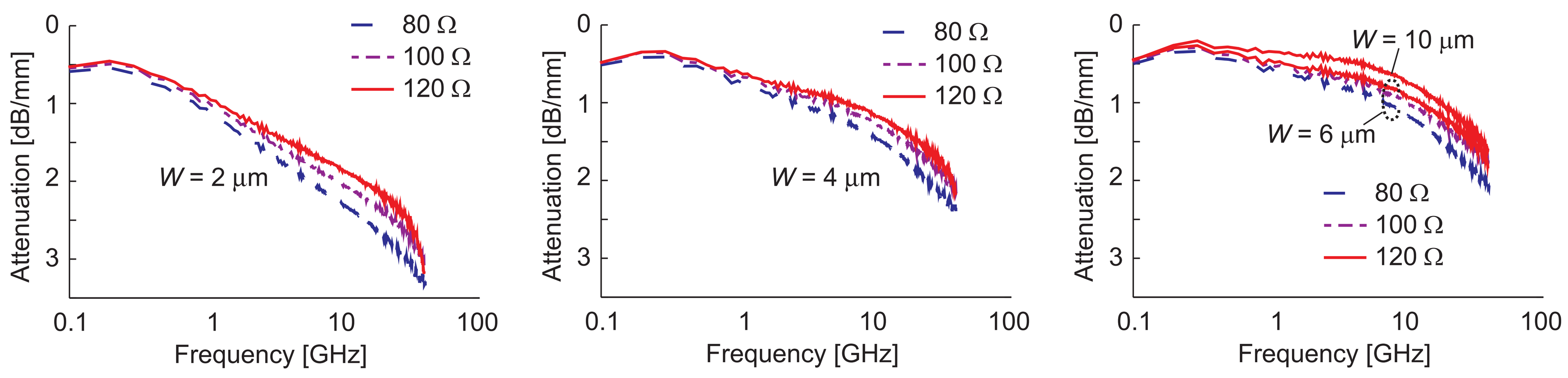
- Type A: DTL (M5)
- Type B: DTL (M5) with underlying metals (M1, M2, M3 and M4)
  L&S of M1, M2, M3 and M4 are 1.0 μm.

Measurement system



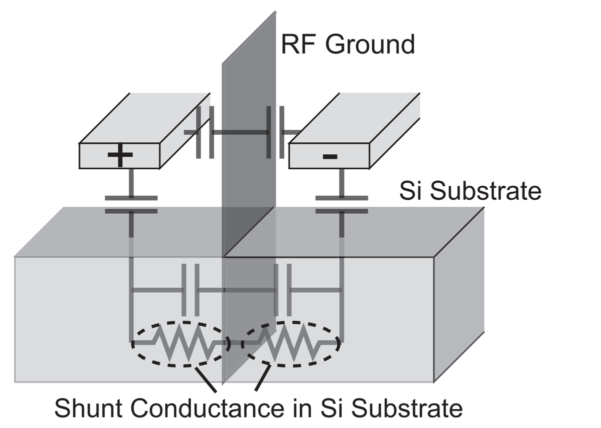
- Vector network analyzer (Agilent, E8364B & N4421B)
- GSGSG type RF probes (Cascade, Infinity)
- SOLT calibration using impedance standard substrate of Cascade
- Pad de-embedding: Open and short patterns

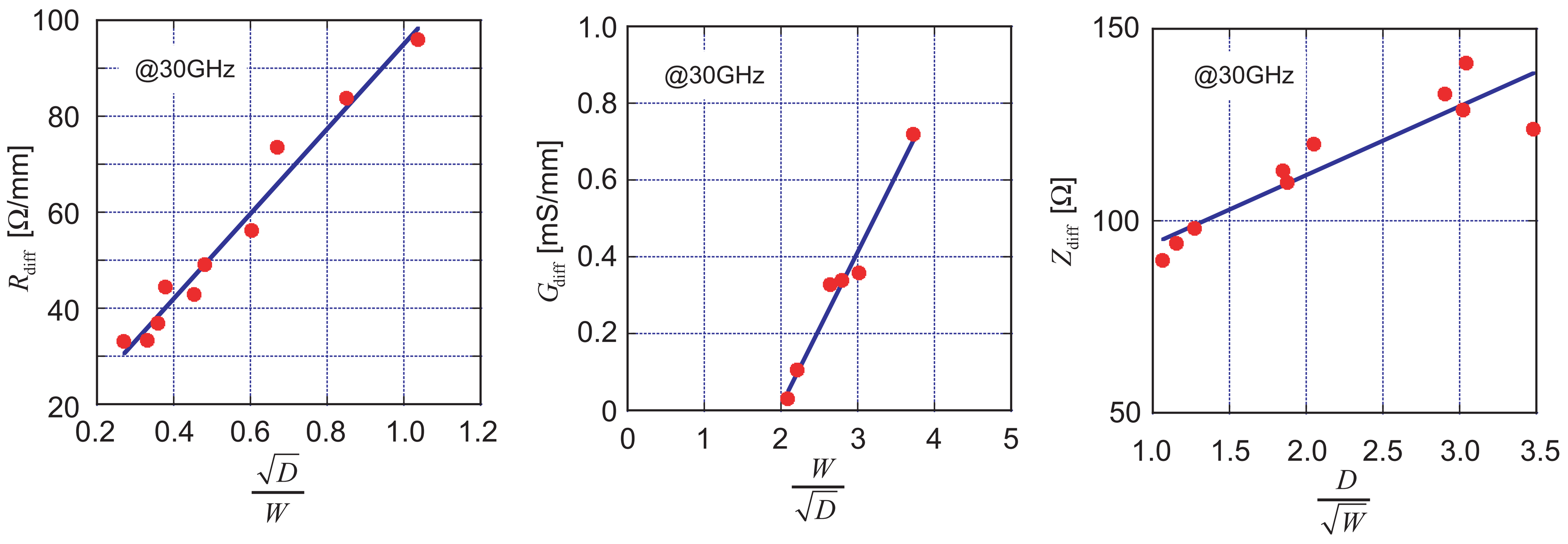
Characteristics



W	*D*	Attenuation	Rdiff	Gdiff	Measured Zdiff
2.0 μm	1.8 μm	3.1 dB/mm	73 Ω/mm	-	98 Ω
4.0 μm	3.7 μm	1.9 dB/mm	49 Ω/mm	31 μS/mm	113 Ω
6.0 μm	2.6 μm	1.9 dB/mm	33 Ω/mm	720 μS/mm	90 Ω
6.0 μm	4.6 μm	1.6 dB/mm	37 Ω/mm	340 μS/mm	110 Ω
6.0 μm	7.4 μm	1.5 dB/mm	43 Ω/mm	107 μS/mm	129 Ω
10.0 μm	11.0 μm	1.4 dB/mm	33 Ω/mm	359 μS/mm	124 Ω

@30GHz





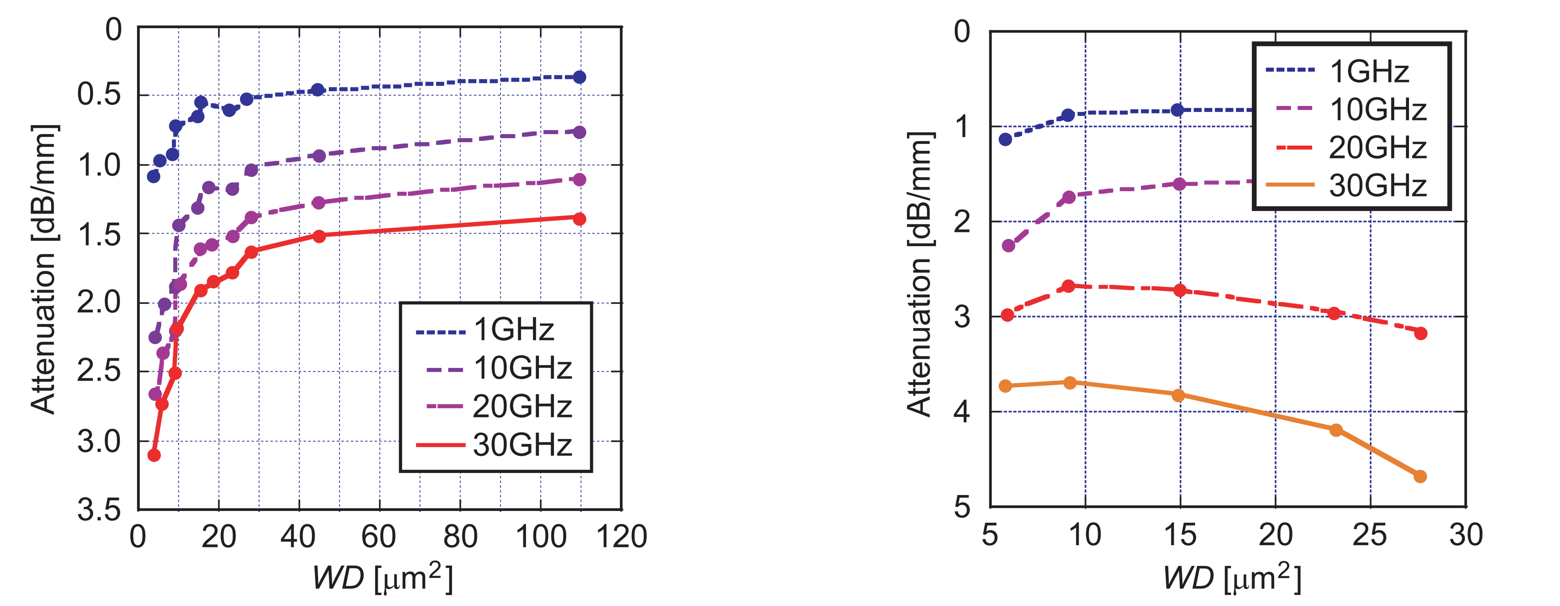
Empirical relationships found

$$R_{diff} \propto \frac{\sqrt{D}}{W}, \quad G_{diff} \propto \frac{W}{\sqrt{D}}, \quad Z_{diff} \propto \frac{D}{\sqrt{W}}$$

Attenuation constant:

$$\alpha \simeq \frac{1}{2}\left(\frac{R_{diff}}{Z_{diff}} + G_{diff} Z_{diff}\right)$$

Attenuation characteristics depend on the *WD* product.



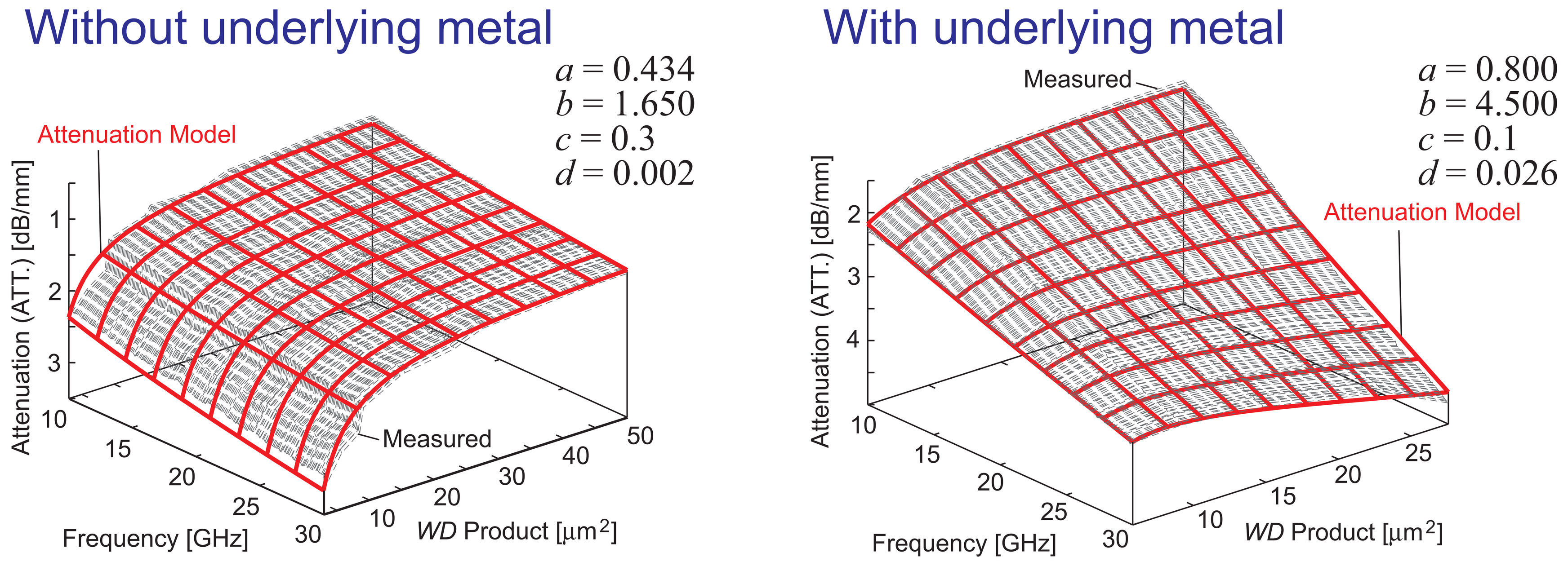
Without underlying metal **With underlying metal**

Attenuation model

Attenuation ATT. can be characterized by a simple function of *WD* [μm²] and frequency *f* [GHz].

$$\text{ATT.} = \underbrace{a + \frac{bf^c}{\sqrt{WD}}}_{\text{Resistive Loss}} + \underbrace{df\sqrt{WD}}_{\text{Dielectric Loss}}$$

Without underlying metal With underlying metal



Conclusions

$$Z_{diff} = g(W, D, f)$$

(Some formulae have been proposed.)

$$\text{ATT.} = h(WD, f)$$

(This Study)

We can design on-chip transmission lines !!