On-Chip Differential-Transmission-Line(DTL) Interconnect for 22nm Technology

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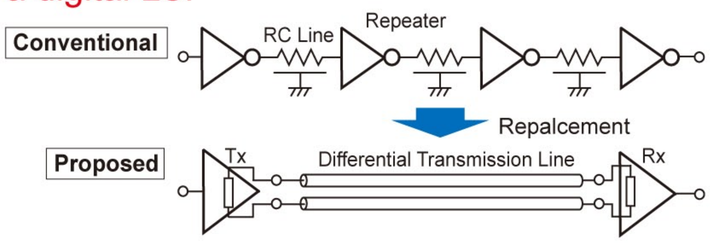
1. Background

Issues for Si LSI:
Delay and Power Dissipation in Long Global Interconnects

Designed as RC lines, Divided by several reqeaters

Transmission Line Interconnect:
- Faster signaling than a conventional RC interconnect
  (Signals can propagate at electromagnetic-wave speed.)
- Power consumption does not depend on a line length.
  (Repeaters are not necessary for high-speed signaling.)

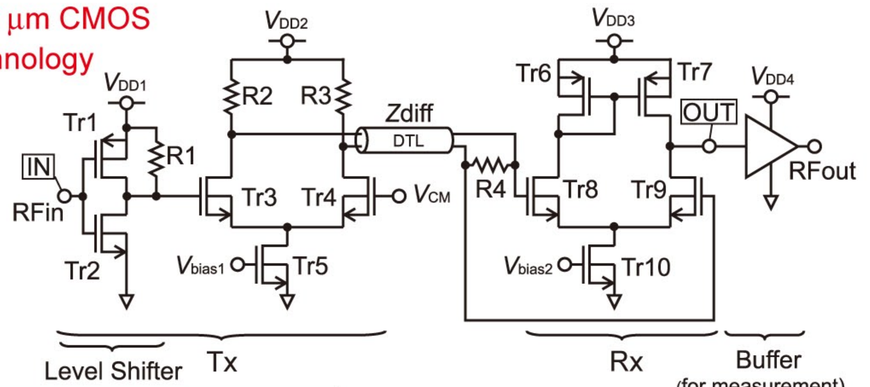
Implementation of high-speed transmission line interconnect to replace global RC interconnect in a digital LSI



Transmission Line, Optical, Wireless, CNT, RC(conventional)

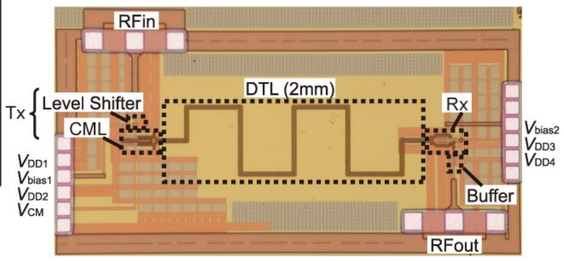
2. On-Chip Differential-Transmission-Line Interconnect

0.18 μm CMOS Technology



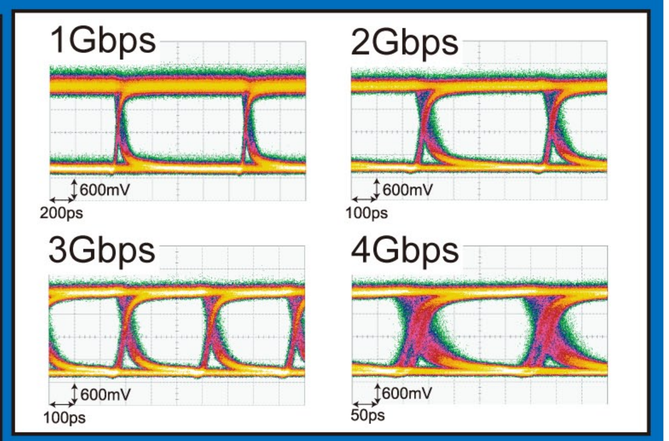
Component	Tr1	Tr2
W / L	10 μm / 0.2 μm	10 μm / 0.2 μm
Component	Tr3, Tr4	Tr5
W / L	310 μm / 0.2 μm	300 μm / 0.4 μm
Component	Tr6, Tr7	Tr8, Tr9
W / L	20 μm / 0.2 μm	20 μm / 0.2 μm
Component	Tr10	
W / L	20 μm / 0.4 μm	

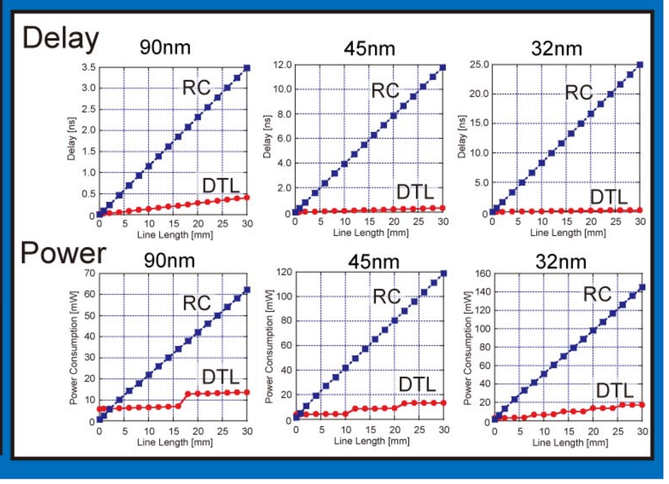
Component	R1	R2	R3	R4
Value	250 Ω	50 Ω	50 Ω	100 Ω
Source	VDD1-4	Vbias1	VCM	Vbias2
Value	1.80 V	1.20 V	1.40 V	0.60 V



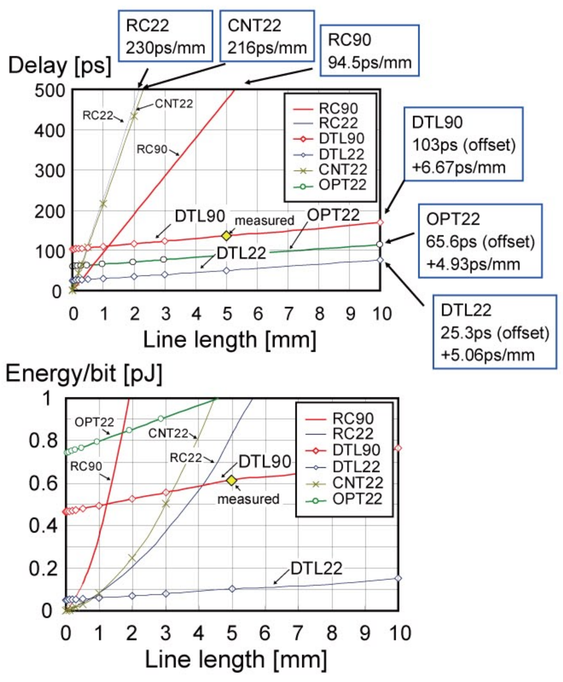
Areas of Tx and Rx are 9700 μm² and 8000 μm².

180nm		90nm	
Max rate:	4Gbps	Max rate:	10Gbps
Power:	9.9mW	Delay:	138ps/5mm
		Power:	2.7mW





3. Performance Evaluation using Figure of Merit (FoM)



RC: conventional repeater-inserted line
DTL: differential transmisttion line
CNT: carbon nano tube
OPT: optical

[1] T. Kuroda, IEICE Trans. 1995

Trade-off between energy *E* and delay *D* [1]

➡ Figure of Merit (FoM)

- High energy achieves small delay.
- Low energy causes large delay.

$$FoM = \frac{\ell^3}{ED} = \frac{\ell^3}{PD^2}$$

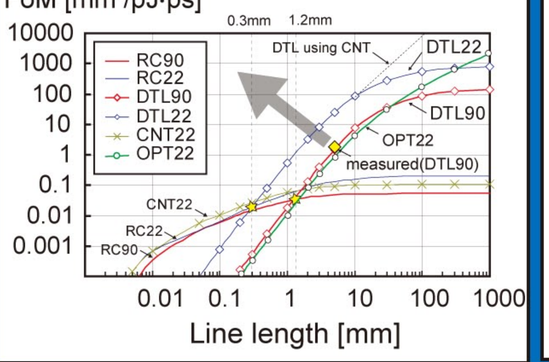
In case of RC interconnect:

$$P \propto \ell, D \propto \ell$$

$$ED = PD^2 \propto \ell^3$$

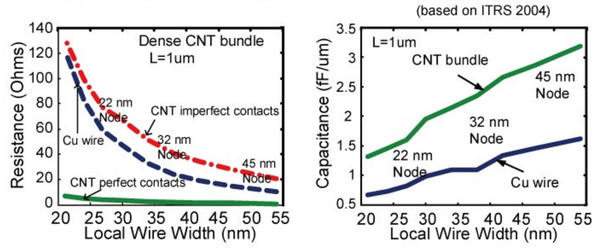
$$FoM \rightarrow \text{const}$$

➡ DTL, OPT, RC, CNT at 90nm and 22nm



CNT vs RC interconencts

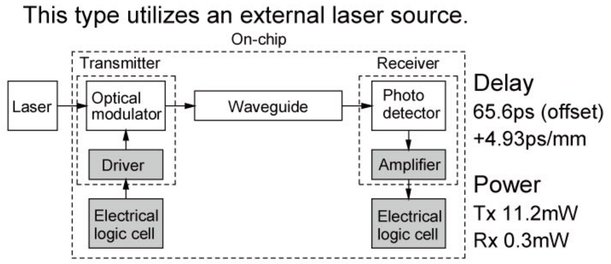
N. Srivastava: ICCAD 2005. (based on ITRS 2004)



Width of global interconnects is assumed to be 2x of half pitch in ITRS 2004.
CNT has lower resistance and larger capacitance than Cu wires.

Optical interconenct

This type utilizes an external laser source.



[6] G. Chen, et al., IITC, 2006.

Delay
65.6ps (offset)
+4.93ps/mm

Power
Tx 11.2mW
Rx 0.3mW

As compared with transmission-line interconnect, delay and power have large offset. It's a big disadvantage as on-chip interconnection.

Delay of TL int.: $\tau_{50\%}^{DTLint} = \tau_{50\%}^{Tx/Rx} + \tau_{50\%}^{DTL}$

Offset-delay of Tx/Rx: $\tau_{50\%}^{Tx/Rx} \propto$ MPU/ASIC 1/2 Pitch

Delay on TL: $\tau_{50\%}^{DTL} = \frac{\ell}{v} \propto \ell\sqrt{\varepsilon_r}$

Delay of RC line: $\tau_{50\%}^{RCint} \propto$ MPU/ASIC 1/2 Pitch $(\ell=0)$

$$\propto \left\{0.4R_{int}C_{int} + 0.7\left(R_{out}C_{int} + R_{out}C_g + R_{int}C_g\right)\right\}\ell \quad (\ell > 0)$$

Power of TL int.: $P_{DTLint} \propto V_{DD}^2$

Power of RC line: $P_{RCint} \propto f(C_g k + C_{int})\ell V_{DD}^2$

# of repeaters: $k \propto \sqrt{\frac{0.4R_{int}C_{int}}{0.7R_{out}C_g}}$

4. Conclusion

- Differential-transmission-line (DTL) can provide a high-speed and low-power interconnect.
- Performance of DTL int. can be scaled as well as Tr. and local interconnects.
- DTL interconnects have superior delay and power performance to RC interconnects at more than 300μm of line length in 22nm process technology.
- The optical interconnect has large offset-delay and power. Important challenges for OPT are improvement of the offset, wire bending, cost.
- CNT is not suitable for long interconnection due to large capacitance. I have some hope to use differential signaling for CNT.