A 6.5-mW 5-Gbps On-Chip DTL Interconnect with a Low-Latency Asymmetric Tx in a 180nm CMOS Technology

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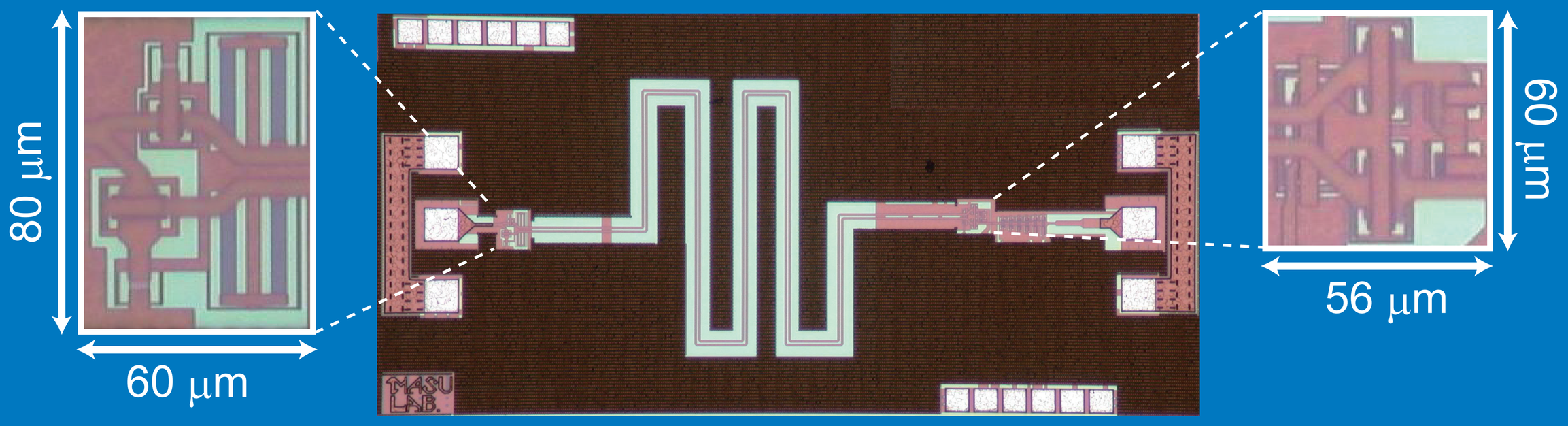


Background

Issues for Si LSI:

Delay and power dissipation in long global interconnects

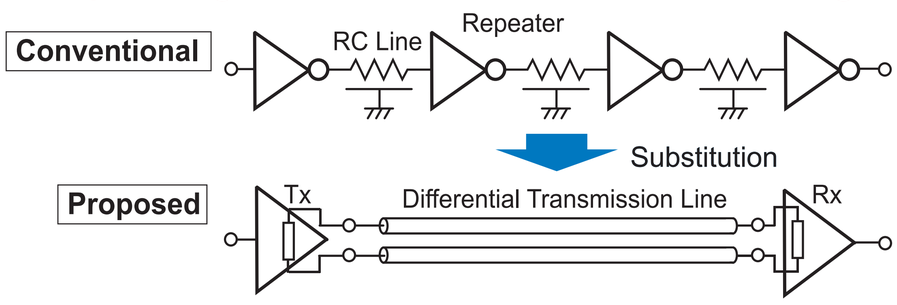
Designed as RC lines, divided by several repeaters

Transmission Line Interconnect:

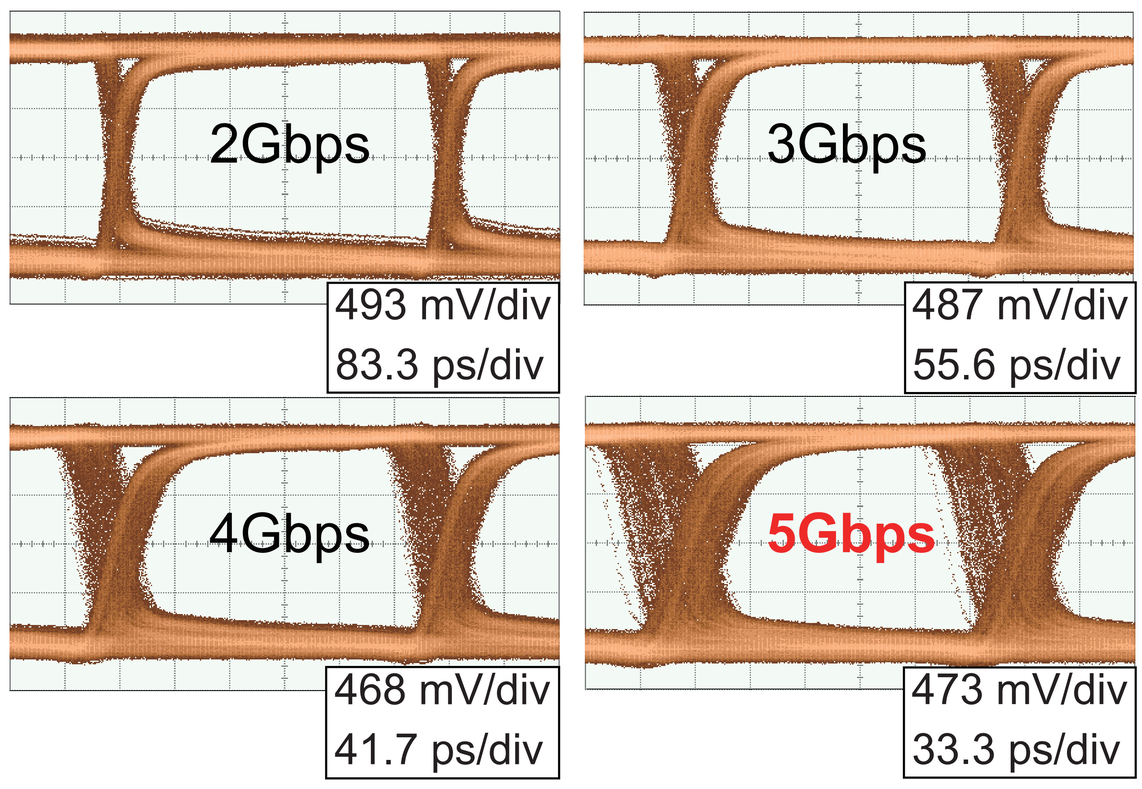
- Faster signaling than a conventional RC interconnect
  (Signals can propagate at electromagnetic-wave speed.)
- Power consumption does not depend on a line length.
  (Repeaters are not necessary for high-speed signaling.)

Purpose of this work

Implementation of high-speed transmission line interconnect IP to replace global RC interconnects in a digital LSI

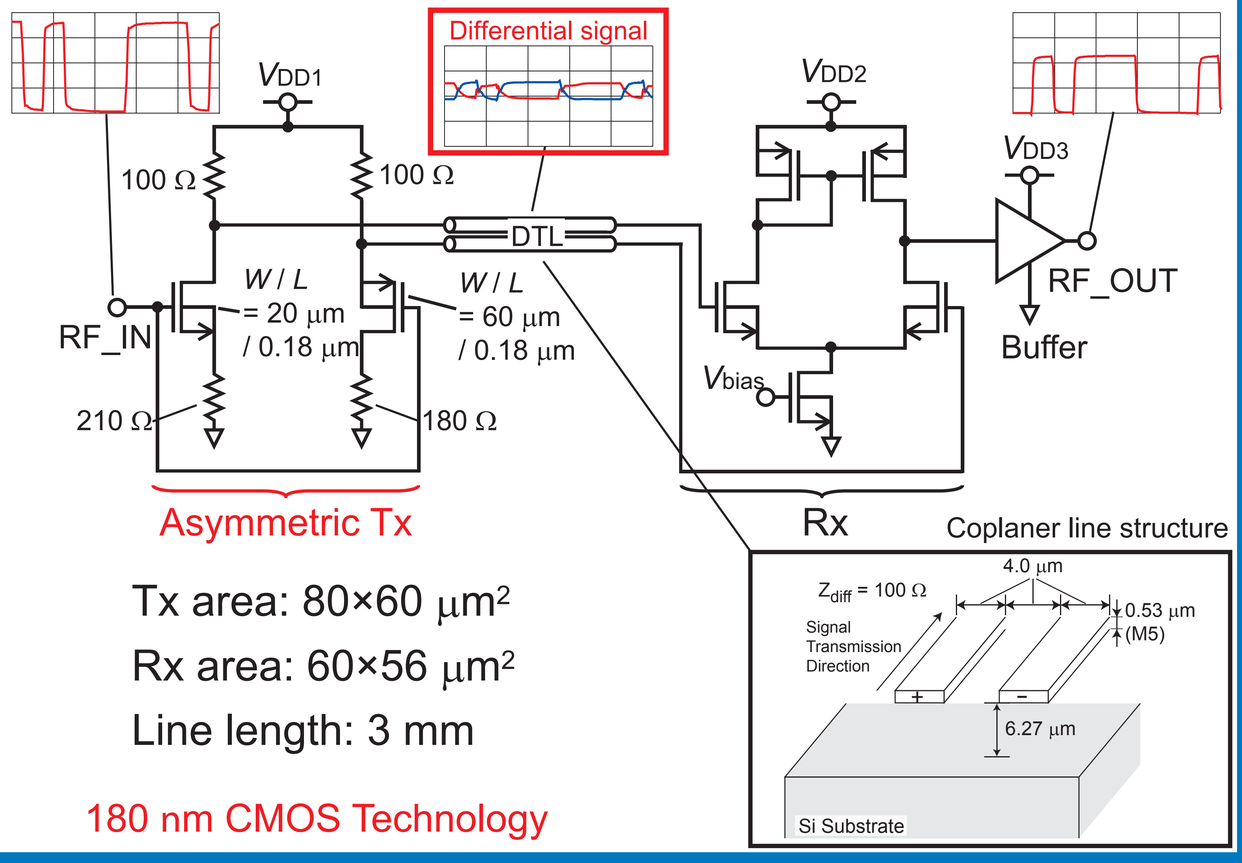


Measured eye patterns



5Gbps signal transmission can be achieved through 3mm line-length interconnect.

Schematic & Operation



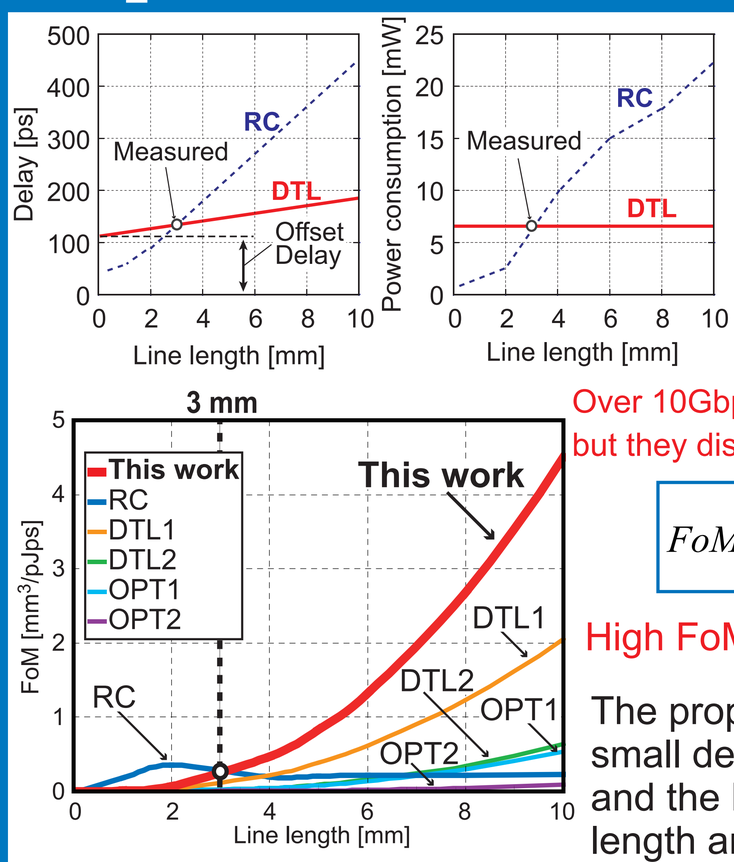
Tx area: 80×60 μm²

Rx area: 60×56 μm²

Line length: 3 mm

180 nm CMOS Technology

Impact



Tx power:	3.5 mW
Rx power:	3.0 mW
Total power:	6.5 mW
Total delay:	140 ps
Tx delay:	52 ps

Over 10Gbps transceivers are already existing, but they dissipate large power **over 100mW**.

$$FoM = \frac{\ell^3}{ED} = \frac{\ell^3}{PD^2}$$

P: Power
D: Delay
E: Energy/bit

High FoM ➡ The interconnect achieves low power & small delay at once.

The proposed interconnect achieves small delay, low power consumption, and the highest FoM at long line length among other techniques.

Conclusion

Maximum 5 Gbps signaling can be achieved using the proposed circuit fabricated by 180 nm COMS technology.

The proposed interconnect has smaller delay and lower power consumption than the conventional RC interconnect over 3 mm.