

# 1D-14 A Multi-Drop Transmission-Line Interconnect in Si LSI

Junki Seita, Hiroyuki Ito, Kenichi Okada, Takashi Sato and Kazuya Masu  
Integrated Research Institute, Tokyo Institute of Technology, Japan

## Background

### Issues for Si LSI:

The delay time and power consumption in global interconnect are the enduring obstacles.

Designed as RC lines, Divided by several repeaters

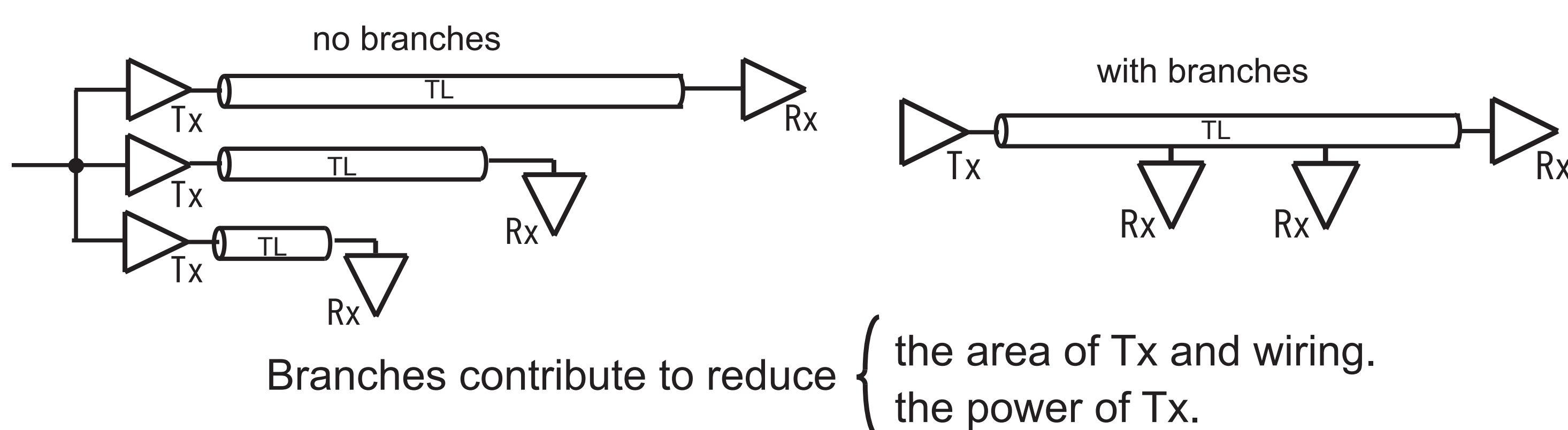
### Transmission Line Interconnect:

- Faster signaling than a conventional RC interconnect (Signals can propagate at high speed.)
- Power consumption does not depend on a line length. (Repeaters are not necessary for high-speed signaling.)

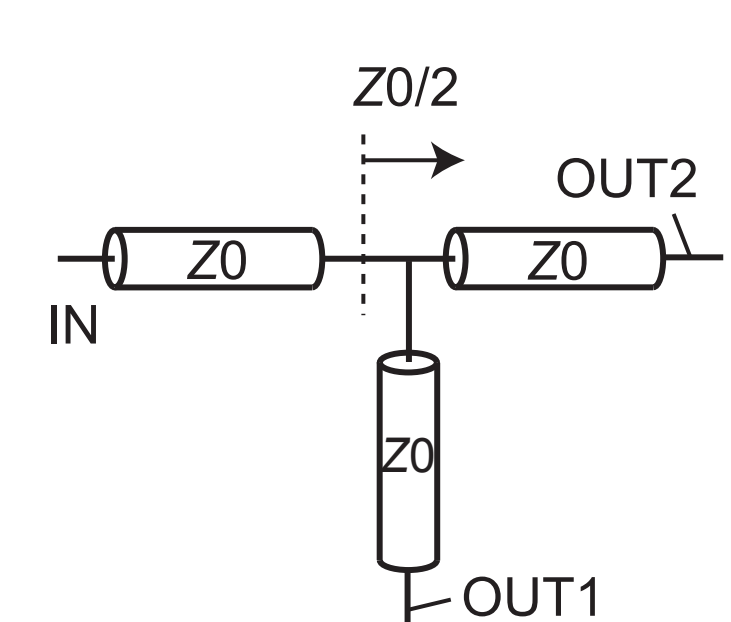
## Purpose

The conventional on-chip TL interconnects are peer-to-peer ones.

**We propose the on-chip TL interconnect with branches.**



## Branching Structures

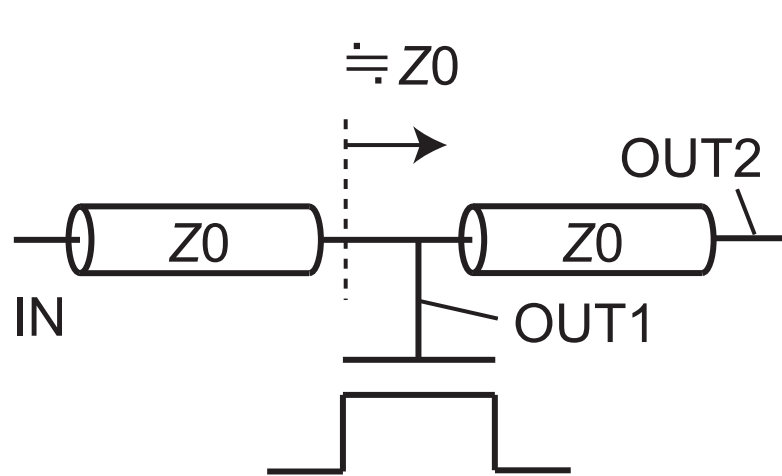


A brute-force branch

※Z0 : characteristic impedance

- Same Z0 in each output line
- Input impedance of parallel transmission-lines becomes half of Z0.

→ Impedance mismatch is caused.



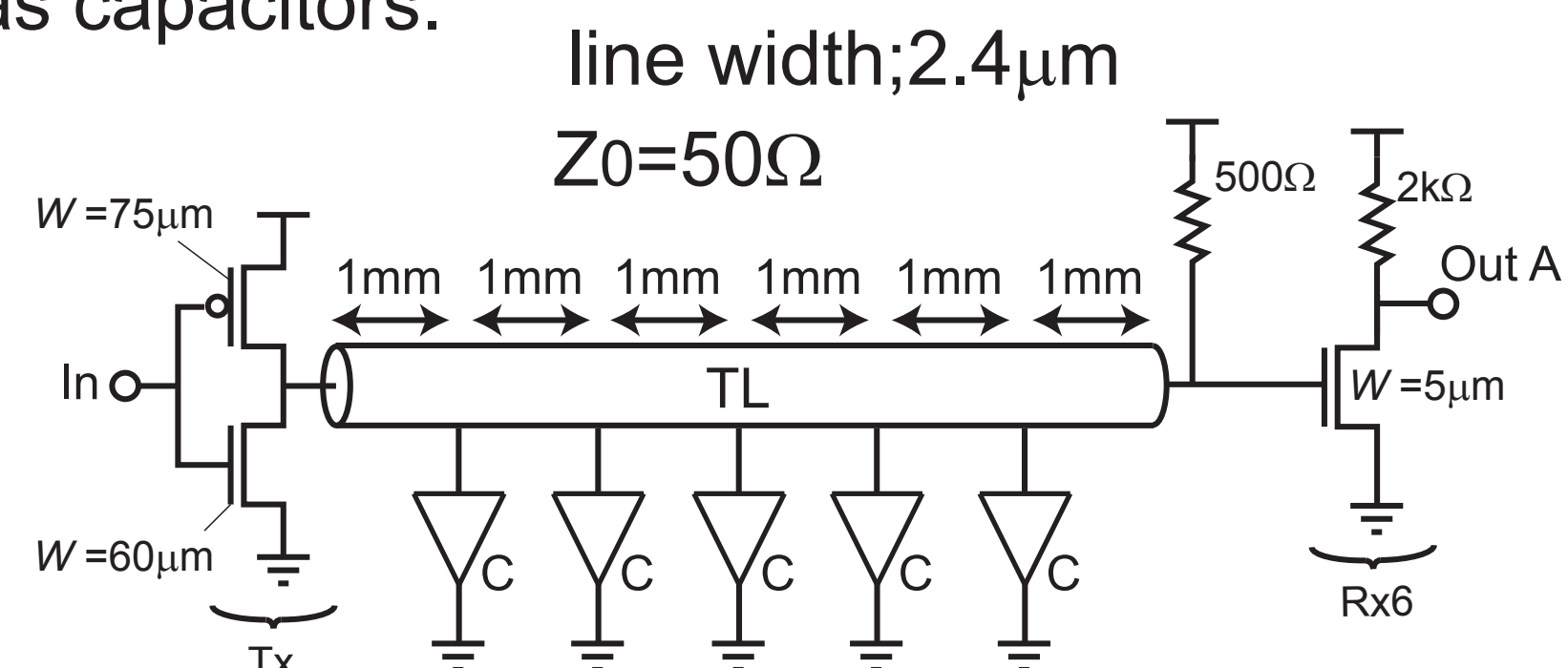
The used structure

- Short branch-line
- Large input impedance of transistor

→ This structure reduce the effect of reflection.

## Test Circuit for Branches

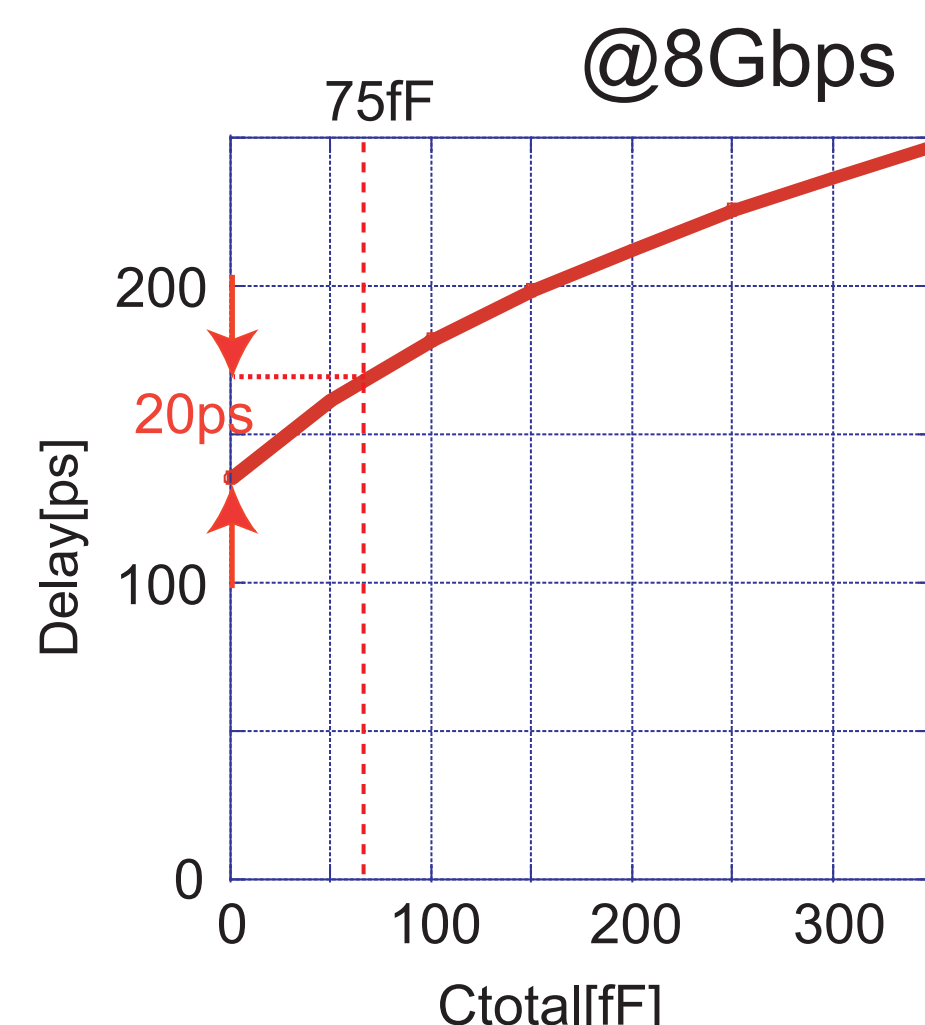
Transistors at branching nodes are modeled as capacitors.



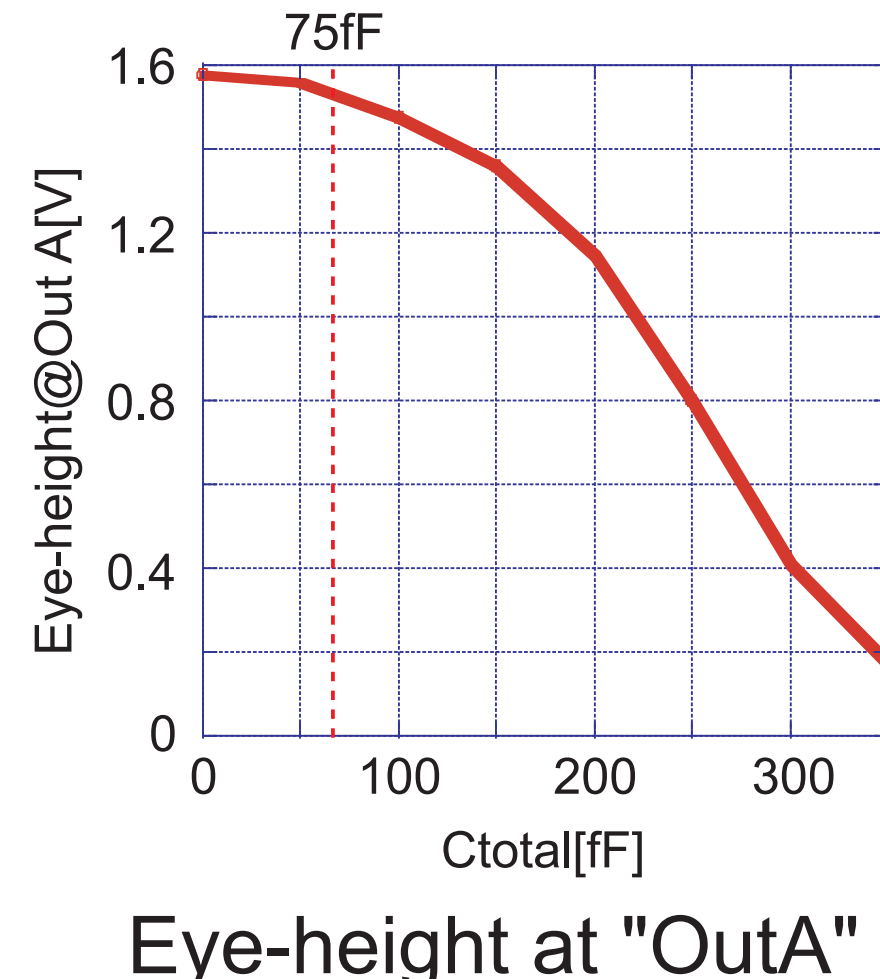
A test circuit to evaluate effects due to gate capacitance of a branching transistor.

- 0.18 μm CMOS process

Simulated by ADS(Agilent).



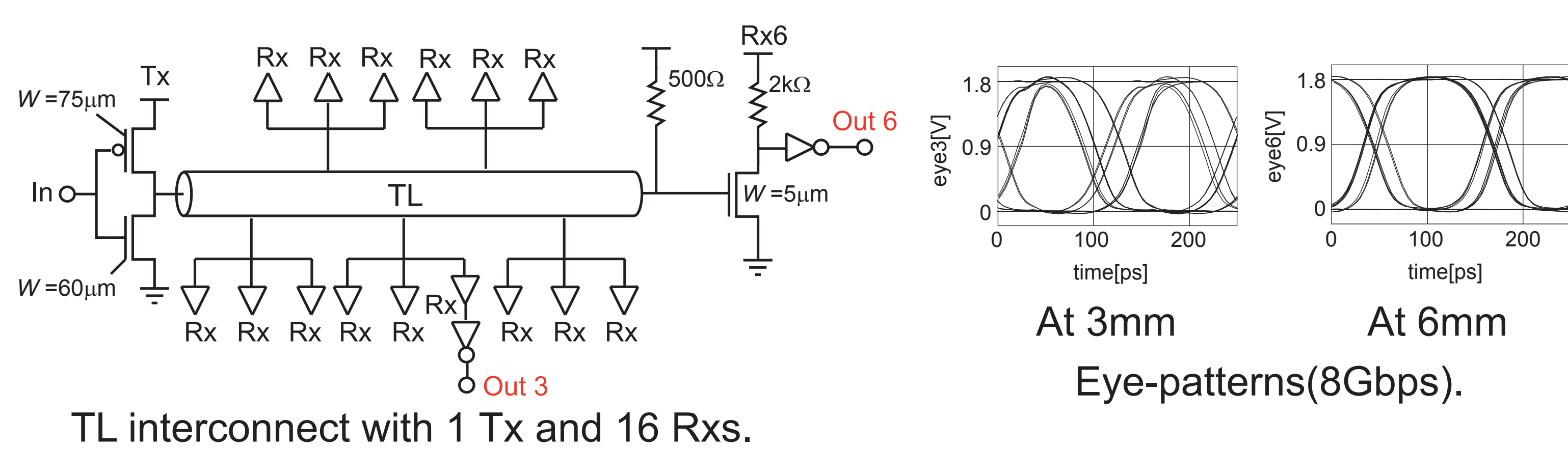
Delay from "In" to "OutA"



Eye-height at "OutA"

- Delay and eye-height degrade as capacitance increases.
- Assumption ; Acceptable degradation of eye-height is 5%.
- 75fF can be connected to the single-ended transmission line. (Then delay is increased by 20ps.)
- Gate widths of Rxs are required to be 5mm for amplifying the signal, and gate capacitance is 5fF in this process.

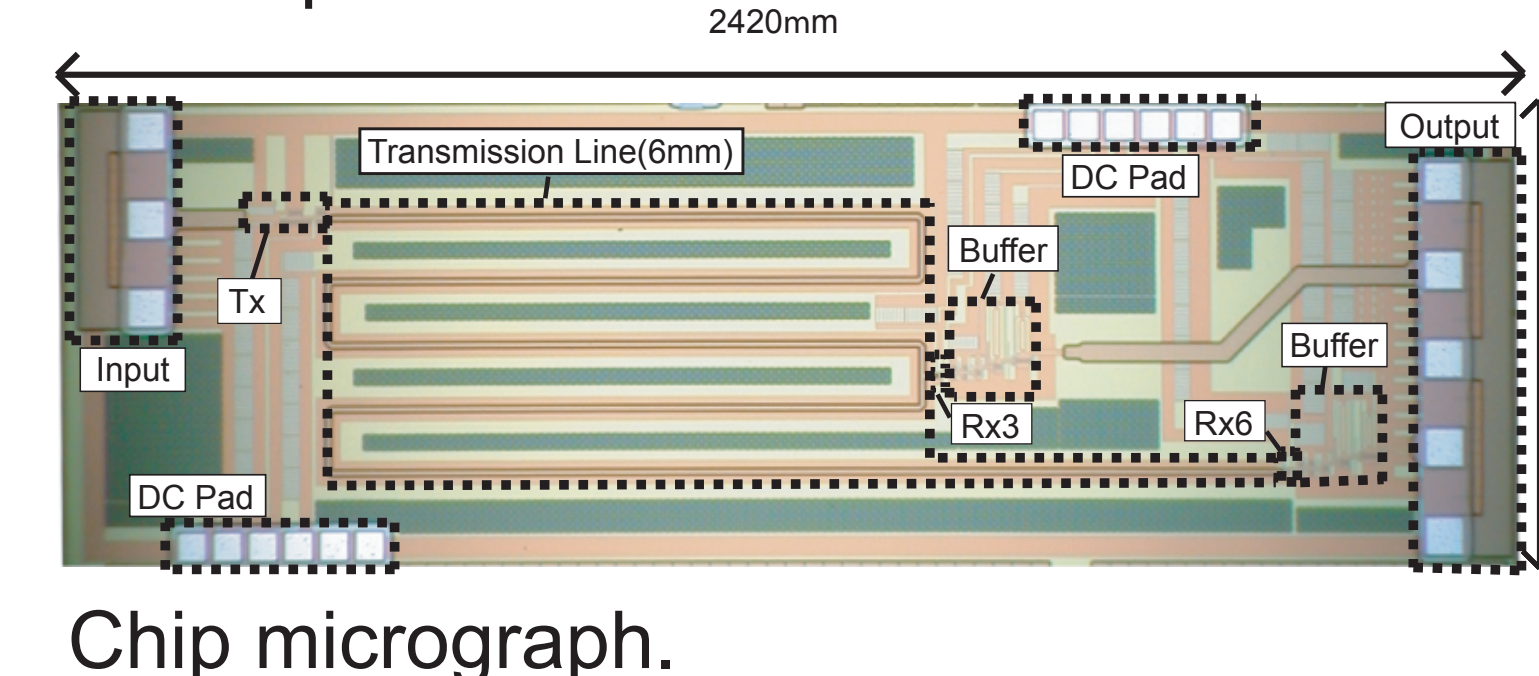
**Thus, sixteen Rxs can be distributed to 6-mm-long TL with limited length of branching lines.**



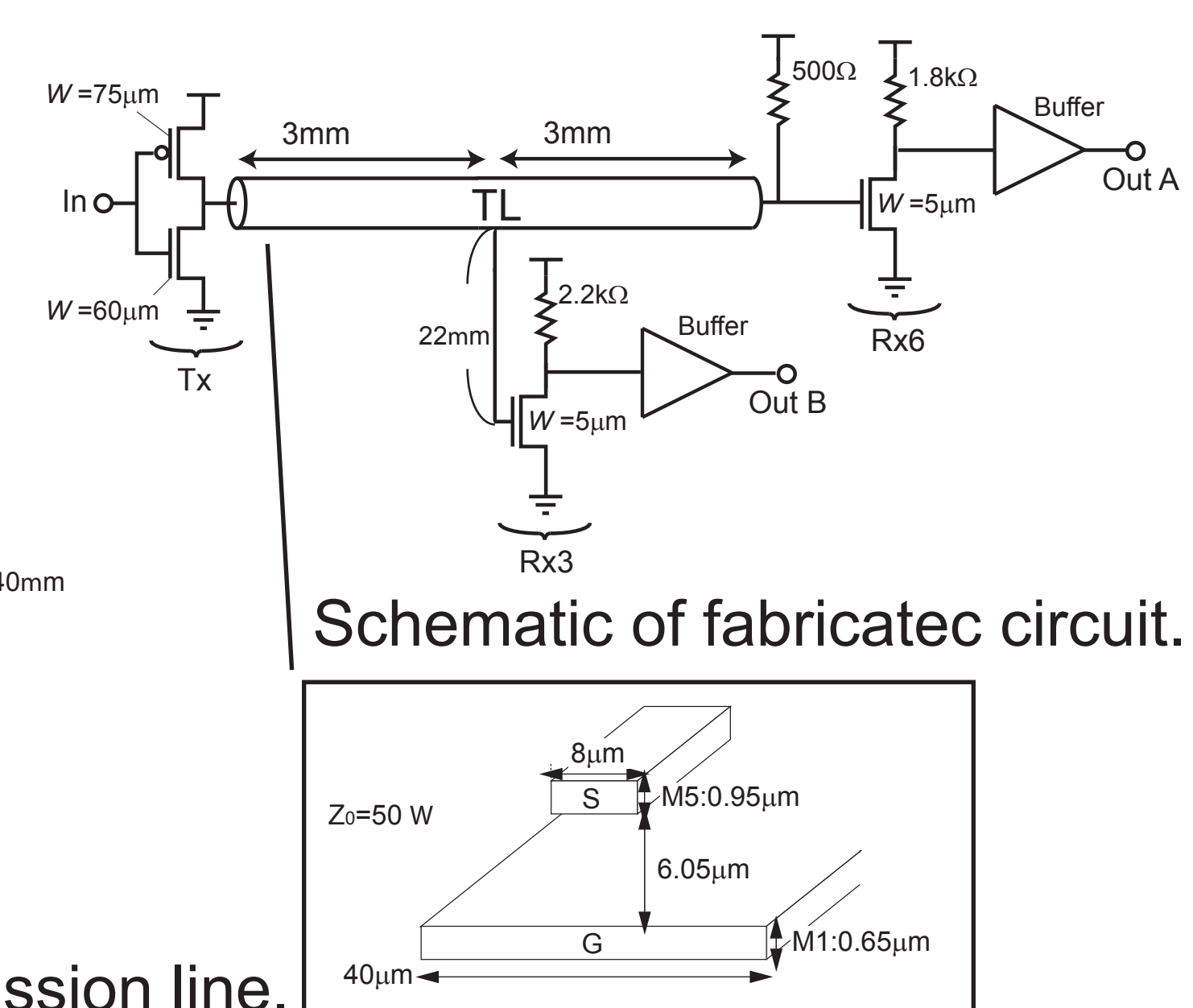
TL interconnect with 1 Tx and 16 Rxs.  
Signals can transmit through the proposed interconnect although deterministic jitter is appeared.

## Schematic & Micrograph

A 6-mm-long TL interconnect with a branch is fabricated by using a 0.18 μm standard Si CMOS process.



Chip micrograph.

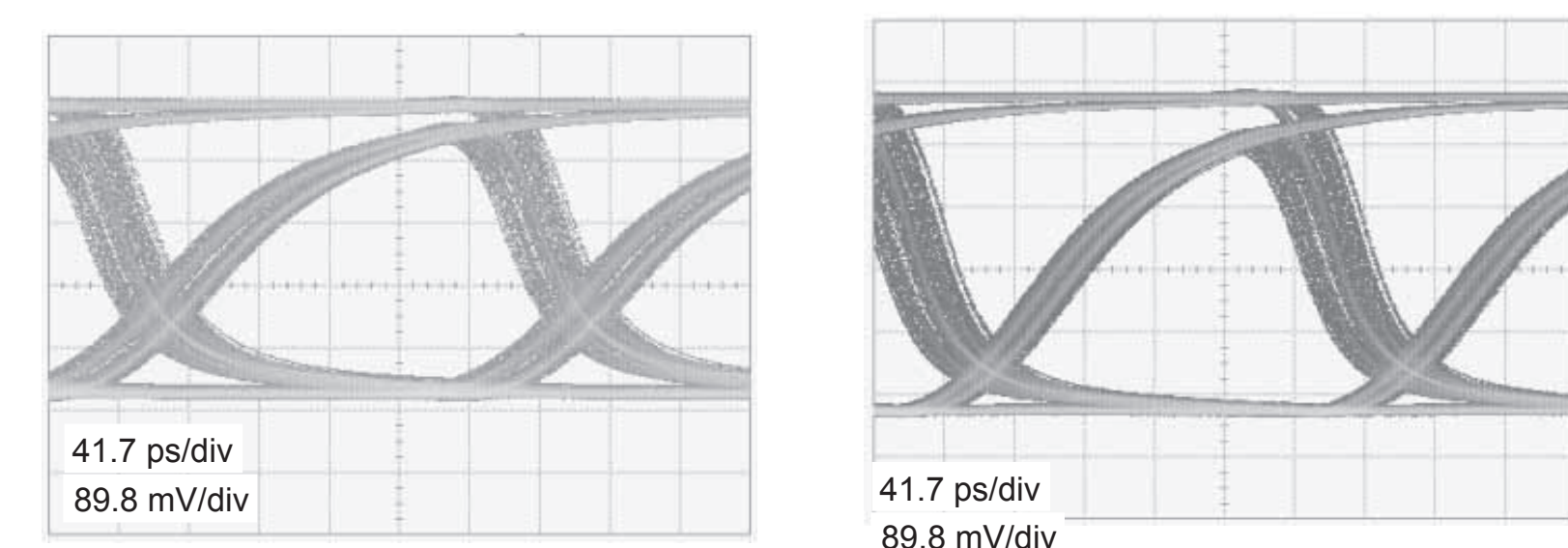


Schematic of fabricated circuit.

Microstrip-type single-ended transmission line.

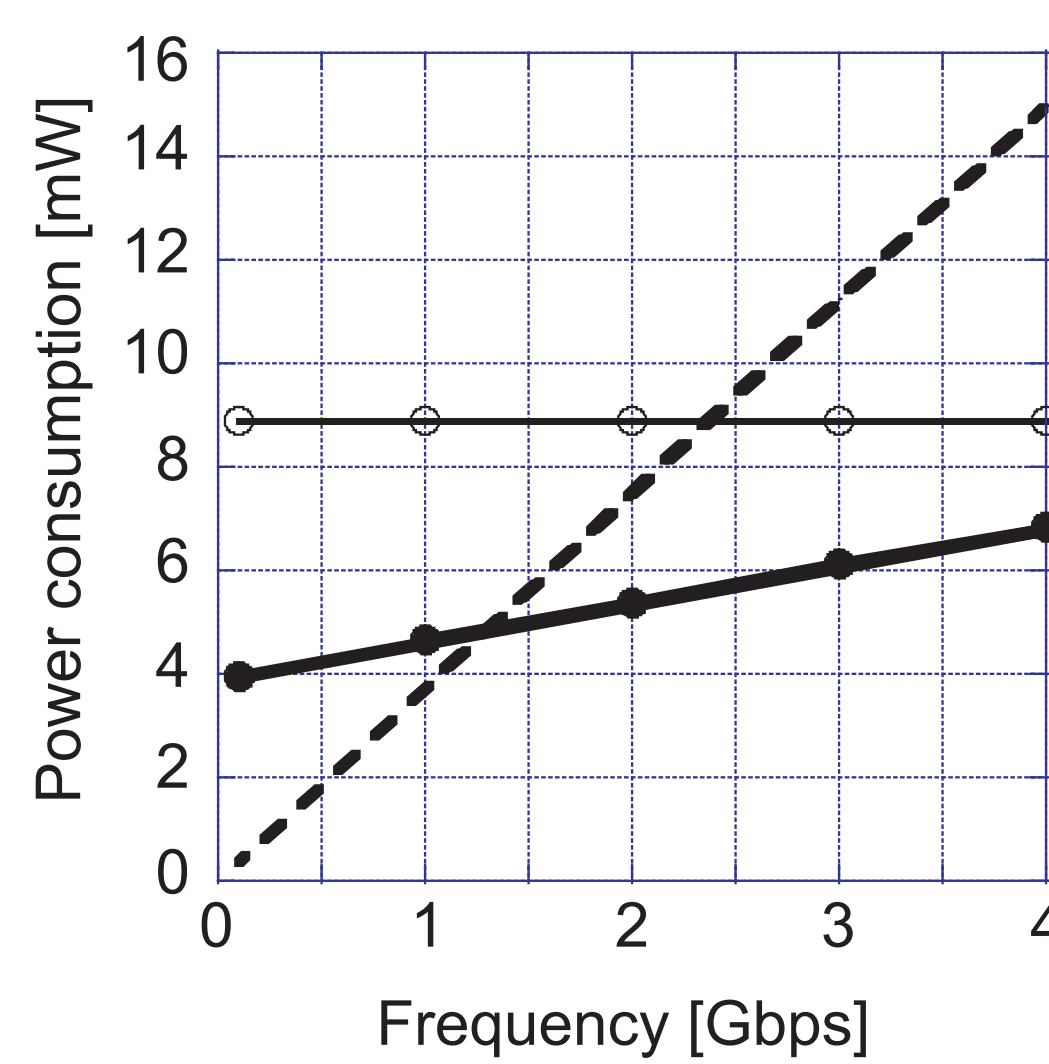
## Measurement Results

investigated by time-domain measurements.



At 3mm  
At 6mm  
Output eye-patterns(4Gbps).

**The proposed TL interconnect with branch can transmit 4Gbps signal.**



Comparison of power consumption.

**The proposed interconnect achieves the lowest power from 1.5 to 4Gbps although it has a branch.**

Delay of existing interconnection scheme.

	Delay[ps@1cm]
The proposed interconnect	144
Differential transmission line interconnect[1]	420
RC Line[3]	500
Modulation[3]	339
Edge-emitting laser[4]	379
VCSEL[4]	446

**The proposed interconnect is fastest.**

## Conclusion

- We have proposed an on-chip transmission-line interconnect with branches.
- In the measurement result, the proposed interconnect realizes 4Gbps signal transmission.
- Transmission line interconnects can improve delay and power of a branching global-interconnect as well as a peer-to-peer interconnect, which will contribute speeding-up and power saving of LSI.