1D-2 LVDS-type On-Chip Transmission Line Interconnect with Passive Equalizers in 90 nm CMOS Process

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Background

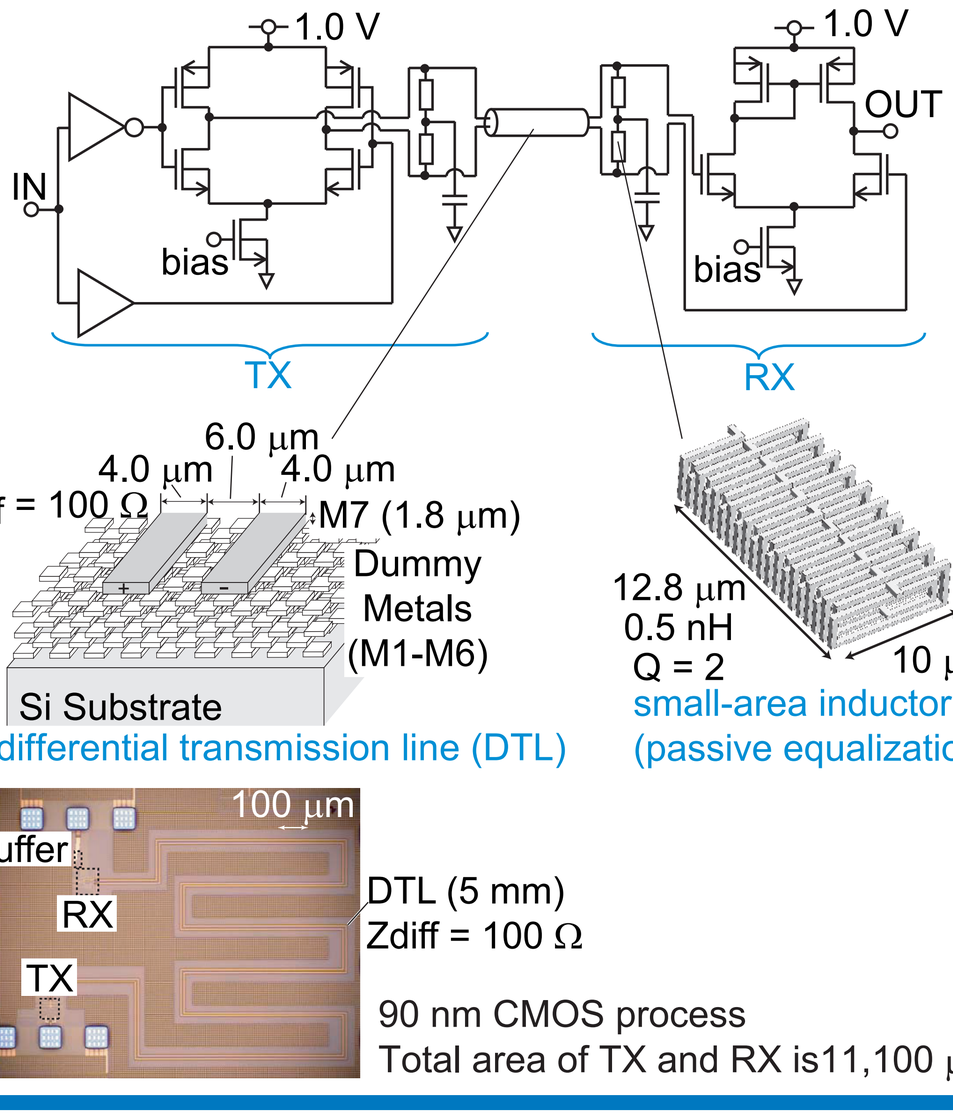
- **Miniaturization of Si CMOS**
  IIncrease in global interconnect delays has complicated timing designs and has limited performances of LSI
- **Transmission line interconnects[1]**
  Much smaller delay than conventional lines
  High power-efficiencies at high-speed signaling

Purpose of this work

To propose a low-voltage-differential-signaling (LVDS) -type transmission line interconnect for achieving higher speed and higher power-efficiency

Transmission line interconnect

Proposed differential transmission line interconnect



differential transmission line (DTL)

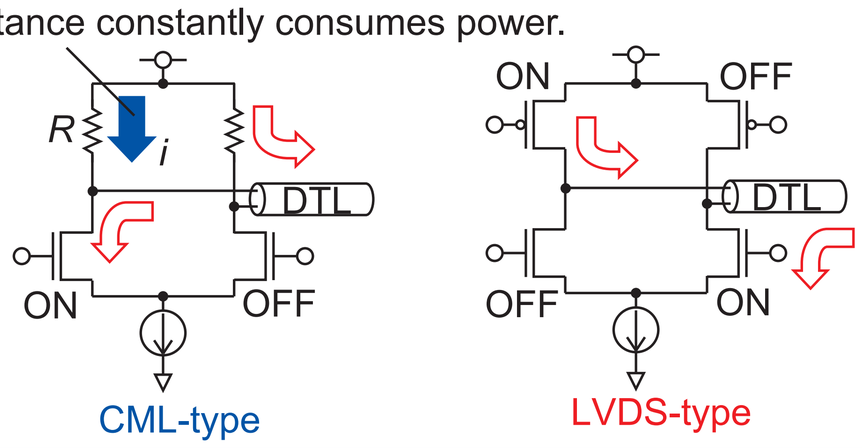
small-area inductor (passive equalization)

DTL (5 mm)
Zdiff = 100 Ω

90 nm CMOS process
Total area of TX and RX is11,100 μm^2

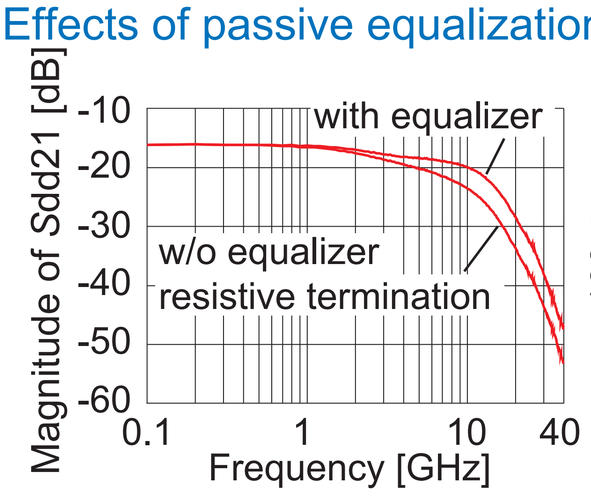
Current flows

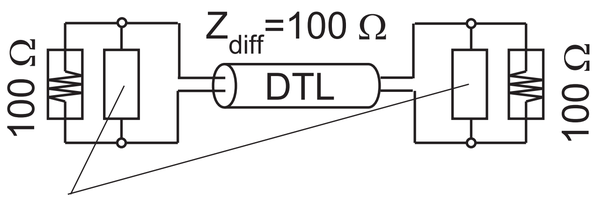
Resistance constantly consumes power.



CML-type LVDS-type

Effects of passive equalization (simulation)

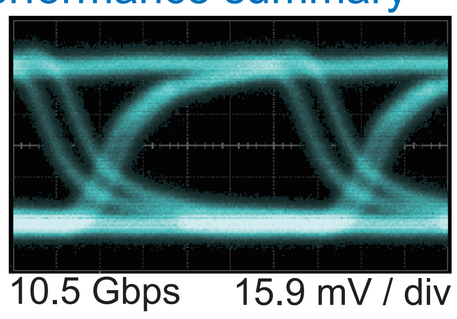




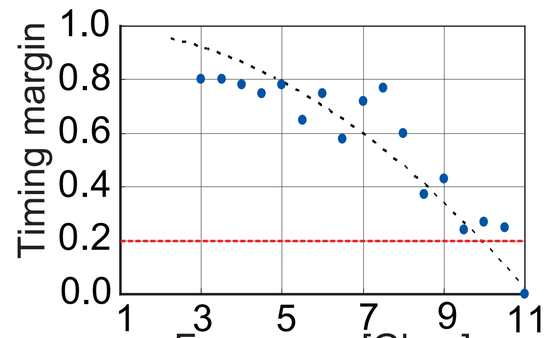
Resister or inductor (100 Ω)

Measurement results

Performance summary



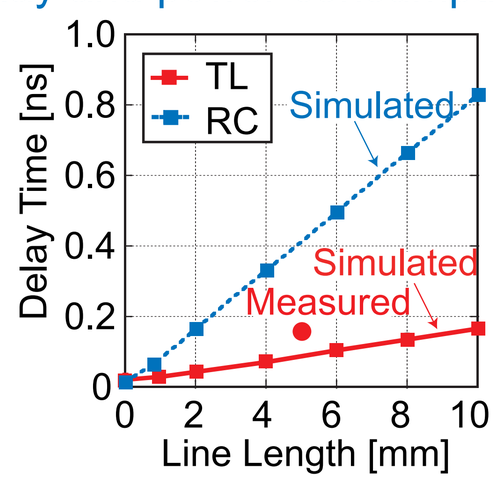
10.5 Gbps 15.9 mV / div 15.9 ps / div

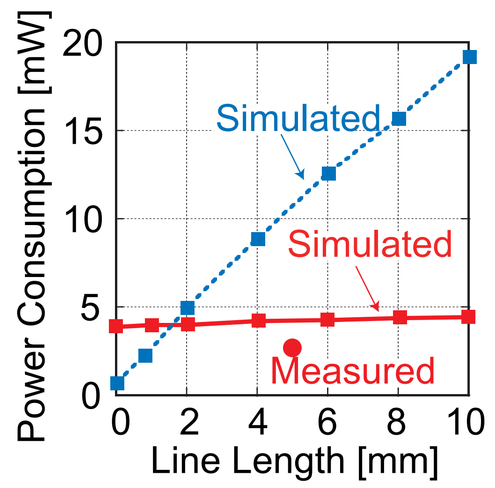


Process	90 nm standard Si CMOS
Maximum frequency	10.5 Gbps
Average delay of 23 chips	173 ps / 5 mm
Power consumption (VDD =1V, 10Gbps)	TX : 1.9 mW , RX : 0.8 mW Total : 2.7 mW
Energy per Bit	0.25 pJ / bit

* Eye-width margin is assumed to be over 20% of period at BER of 10^{-12}.

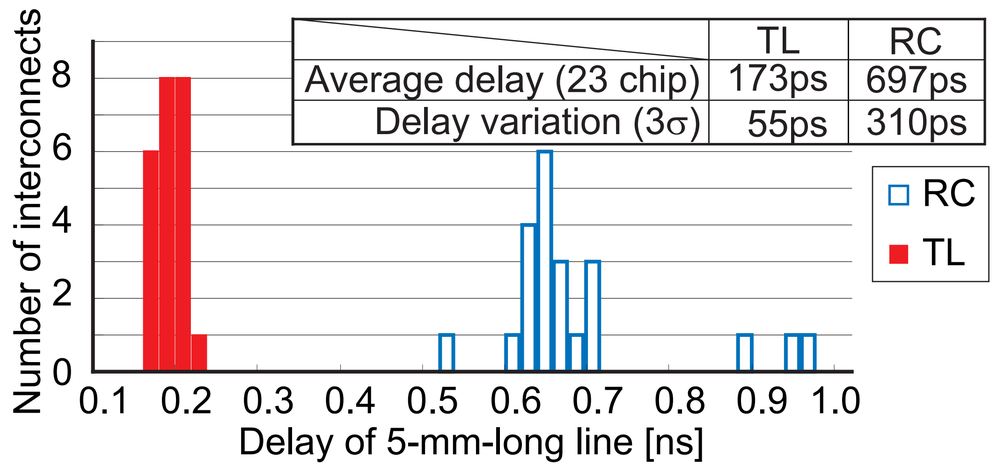
Delay and power consumption





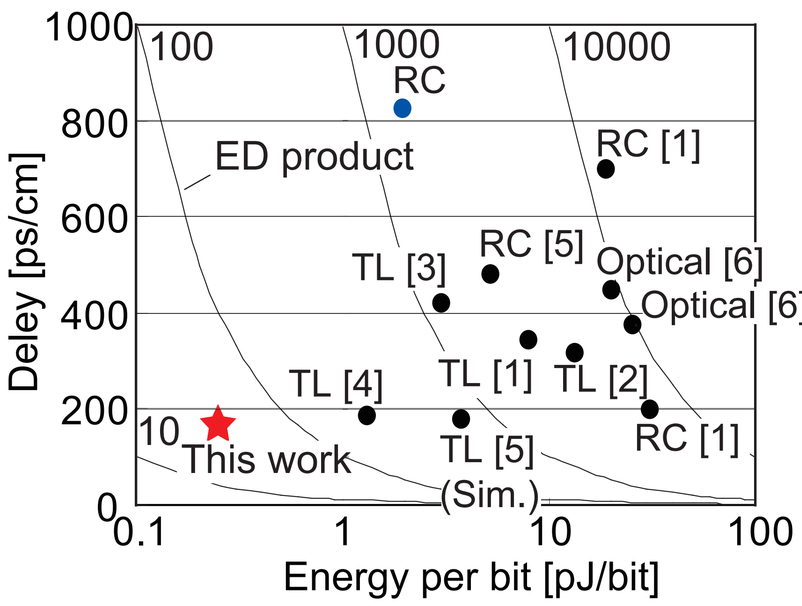
RC line: Minimum line widths and optimal repeater spacing (0.4mm)

Measured delay variation



	TL	RC
Average delay (23 chip)	173ps	697ps
Delay variation (3σ)	55ps	310ps

Conclusion



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- The LVDS-type on-chip transmission line interconnect was proposed.
- Delay of the proposed transmission line interconnect is among the shortest, and energy per bit is the best in reported on-chip long-interconnects.