A Low-Power Differential Transmission Line Interconnect using Wafer Level Package Technology

Tomoaki Maekawa[1], Takahiro Ishii[1], Junki Seita[1], Hiroyuki Ito[2], Kenichi Okada[1], Hideki Hatakeyama[3], Yusuke Uemichi[3], Takuya Aizawa[3], Tatsuya Ito[3], Ryozo Yamauchi[4] and Kazuya Masu[1]

[1]Integrated Research Institute, Tokyo Institute of Technology, [2]Precision and Intelligence Laboratory, Tokyo Institute of Technology, [3]Electron Device Laboratory, Fujikura Ltd., [4]Fujikura Ltd., Japan

Background

Miniaturization of Si CMOS

Increase of global interconnect delay

Solution:

On-chip Transmission line interconnects[TLI][1-7]

Advantages

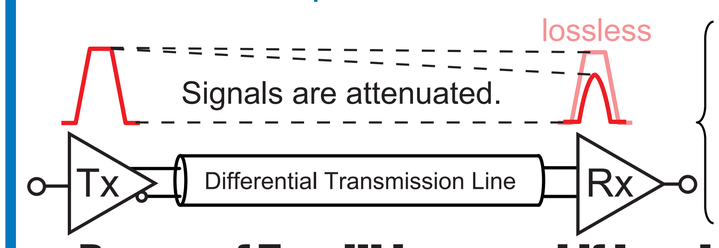
- Near-speed-of-light signaling
- Repeater less : low power consumption

[1]R.T.chang, *et al.*, JSSC, 2006. [2]H.Ito, *et al.*,IEDM 2004.[3]S.Gomi, *et al.*, CICC, 2004. [4]H.Ito, *et al.*, ASSCC, 2005.[5]T.Ishii, *et al.*, ASSCC, 2006. [6]H.Ito, *et al.*, IITC, 2007. [7]H.Ito, *et al.*, VLSI, 2007.

Challenge&Purpose

Issue: Large attenuation due to large resistance of transmission lines

Power consumption of TLIs is almost determined by static power of a Tx and an Rx.



Tx in conventional TLIs has to output large-amplitude signals for compensating large loss.

Rx in conventional TLIs need to have large gain for amplifying small input-signals.

Power of Tx will be saved if low-loss transmission line can be achieved.

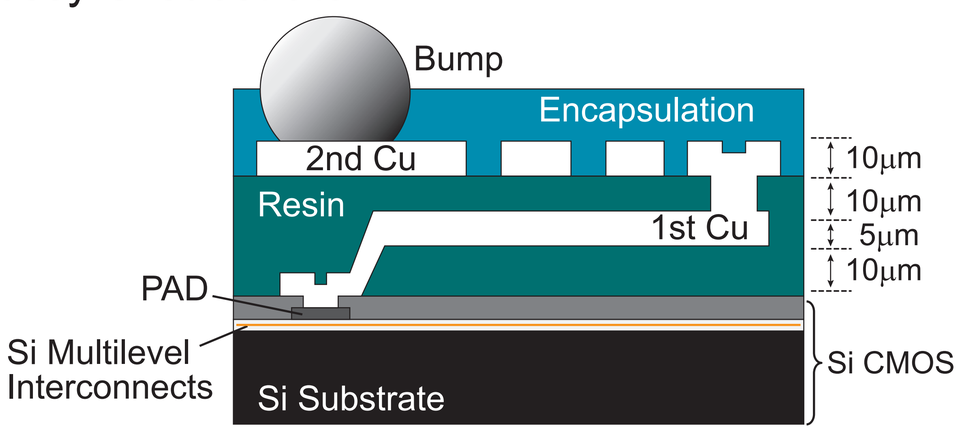
Purpose

To develop low-power TLIs with low-loss transmission lines in wafer level package process.

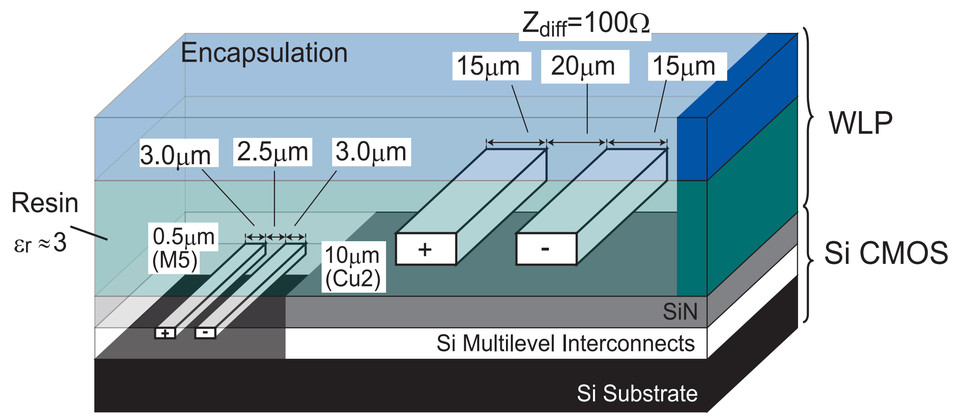
Wafer Level Package (WLP)

Wafer Level Package Technology

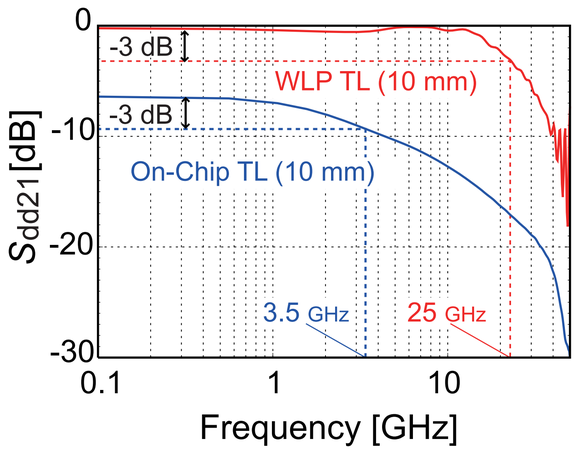
- Low resistive lines due to thick metal layers.
- Induced eddy currents in a Si substrate can be reduced because thick resin layers separate metal layers from a lossy Si substrate.



Structures of transmission lines



Comparison of measured signal attenuation

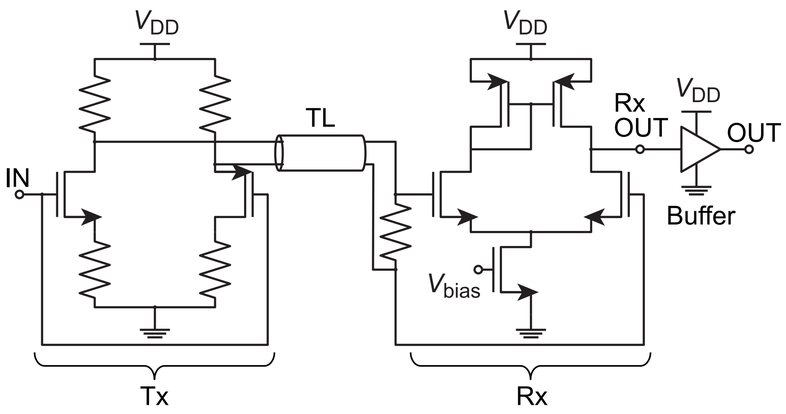


Process	DC resistance	Attenuation
CMOS	125 Ω/cm	7.3 dB/cm
WLP	0.8 Ω/cm	0.5 dB/cm

@1.5 GHz

Low-loss transmission lines can be achieved by using WLP.

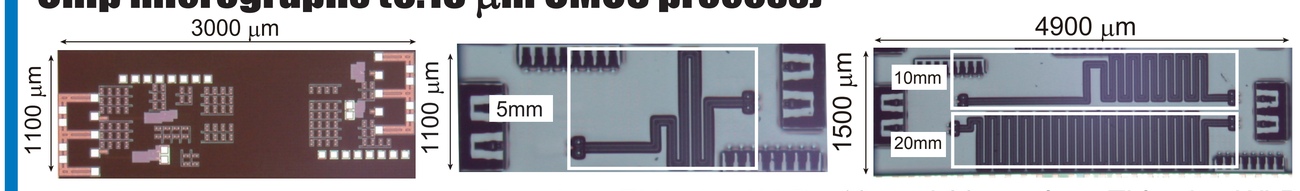
Schematic of a TLI



Tx consists of a NMOS source degeneration and a PMOS source follower for generating differential signals [5].

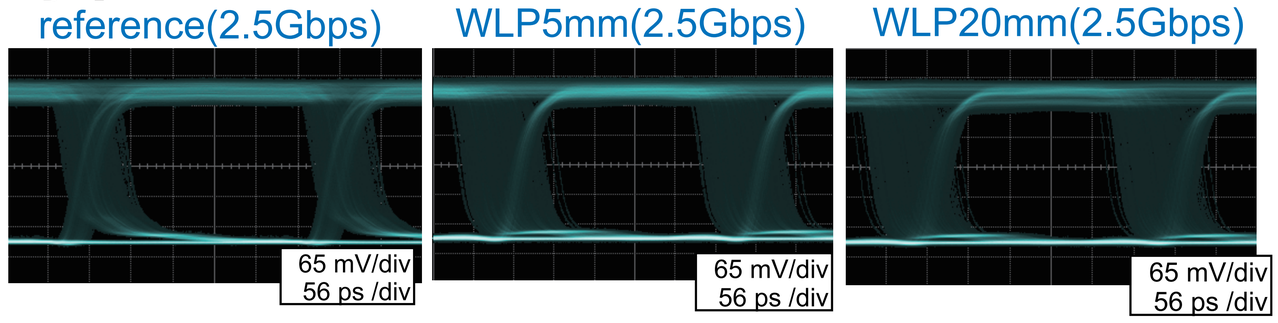
Measurement Results

Chip micrographs (0.18 μm CMOS process)



The conventional TLI(reference) | 5-mm-long TLI using WLP | 10- and 20-mm-long TLI using WLP

Eye patterns



Performance summary

●5-mm-long TLIs

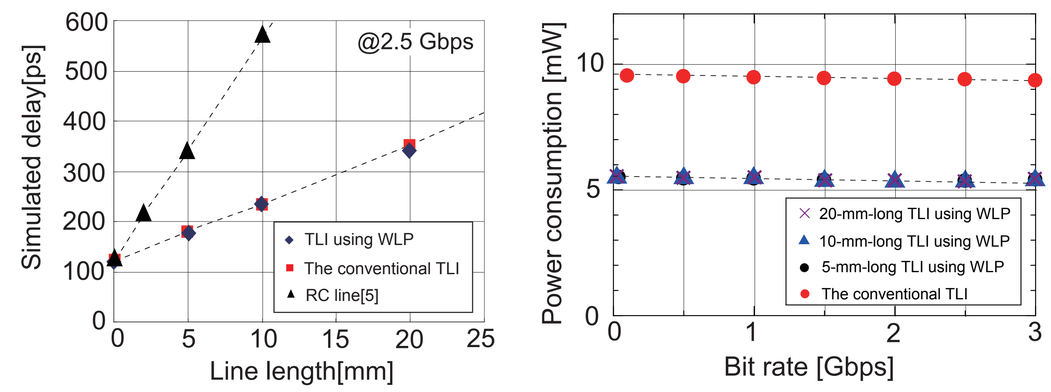
Technology	0.18μm Si CMOS	0.18μm Si CMOS WLP
Delay[Sim.]	180 ps	178 ps
Power Consumption @3Gbps	Tx : 6.5 mW(1.2 V) Rx : 3.1 mW(1.8 V) total : 9.5 mW	Tx : 4.1 mW(1.2 V) Rx : 1.3 mW(1.8 V) total : 5.5 mW
Area	Tx : 90 × 140 μm² Rx : 80 × 50 μm²	Tx : 85 × 120 μm² Rx : 80 × 50 μm²
Maximum bit rate	4.5 Gbps	3.5 Gbps

●10- and 20-mm-long WLP TLIs

Line length	10 mm	20 mm
Technology	0.18μm Si CMOS WLP	
Delay[Sim.]	232 ps	350 ps
Power Consumption @2.5 Gbps	Tx : 4.0 mW(1.2 V) Rx : 1.2 mW(1.8 V) total : 5.2 mW	Tx : 4.1 mW(1.2 V) Rx : 1.4 mW(1.8 V) total : 5.5 mW
Area	Tx : 85 × 120 μm² Rx : 80 × 50 μm²	Tx : 85 × 120 μm² Rx : 80 × 50 μm²
Maximum bit rate	2.6 Gbps	3.4 Gbps

Maximum bit rate is determined by eye-width.
Eye-width margin is assumed to be over 20 % of period at BER of 10^{-12}.

Discussions with delay and power consumption



- Simulated delay of TLIs using WLP linearly increase as line length increases.
- The proposed TLI has almost the same delay as the conventional TLI.
- Power of TLIs hardly depends on bit rates and line length.
- TLIs using WLP achieve 42% smaller power than conventional TLIs.

Conclusions

- A low power on-chip TLI using WLP technology is developed.
- Proposed TLIs using WLP had smaller power consumption than that using only CMOS process.
- Unique design strategies for on-chip TLIs using WLP would be required for achieving higher-speed signaling.