An Over-12-Gbps On-Chip Transmission Line Interconnect with a Pre-Emphasis Technique in 90 nm CMOS

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Background

High-performance LSI

Multiple circuit block configuration

On-chip interconnects among circuit blocks

Parallel interconnection → Serial interconnection

Key issues: Wideband, low latency and low power consumption

Purpose

High-speed on-chip signaling

- Differential transmission line
- Pre-emphasis transmitter circuit
  Small circuit area and low power operation

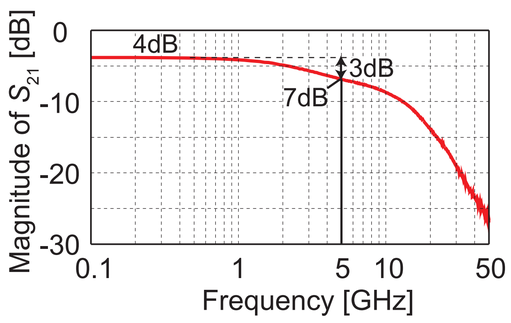
Pre-emphasis Technique

Signal quality is degraded at high-frequency because of the skin effect.

→ Compensation techniques for frequency dependence of transmission line loss

- Tx side: Pre-emphasis
- Rx side: Equalization

Rising and falling edges of Tx output are pre-emphasized.



Characteristics of an on-chip transmission line.
The line length is 5 mm.

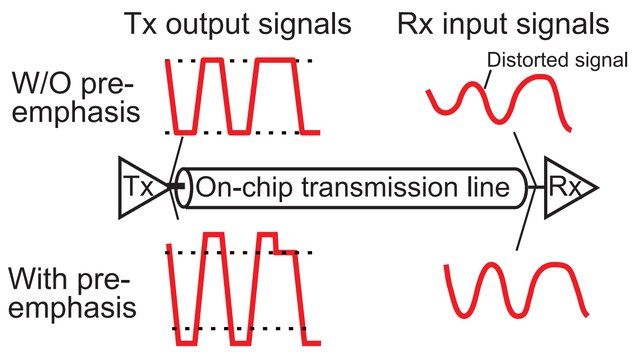
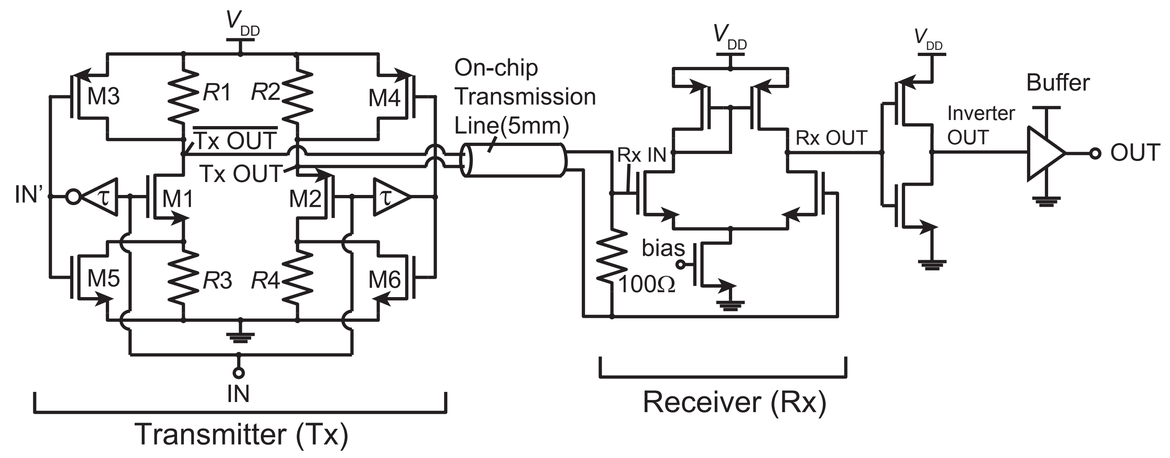
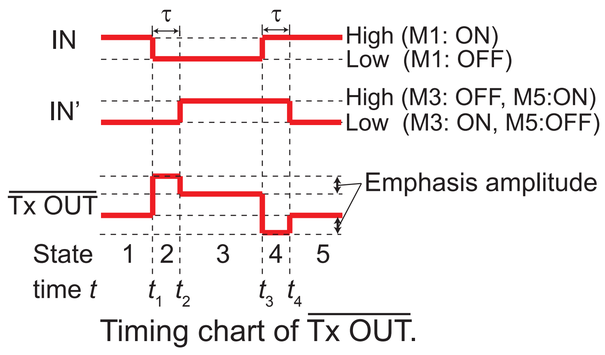


Image of a pre-emphasis effect.

Circuit Operation



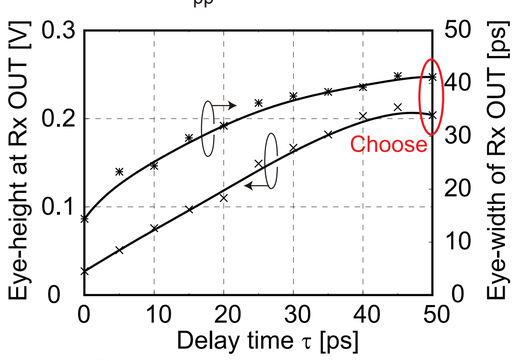


Timing chart of $\overline{\text{Tx OUT}}$.

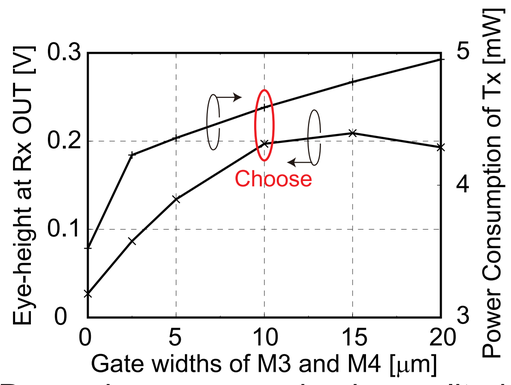
State1 ($t<t_1$) IN is High, $\overline{\text{Tx OUT}}$ is Low.
State2 ($t_1 \le t<t_2$) IN is Low, $\overline{\text{Tx OUT}}$ is High.
State3 ($t_2 \le t<t_3$) IN' is High (M3:OFF, M5:ON).
The rising edge is emphasized.
State4 ($t_3 \le t<t_4$) IN is High, $\overline{\text{Tx OUT}}$ is Low.
State5 ($t_4 \le t$) IN' is Low (M3:ON, M5:OFF).
The falling edge is emphasized.

Design

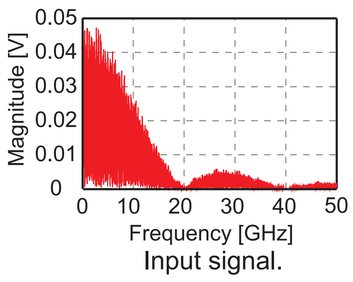
Input signal: 1.0V_{pp}, PRBS; 2^9-1, 20Gbps



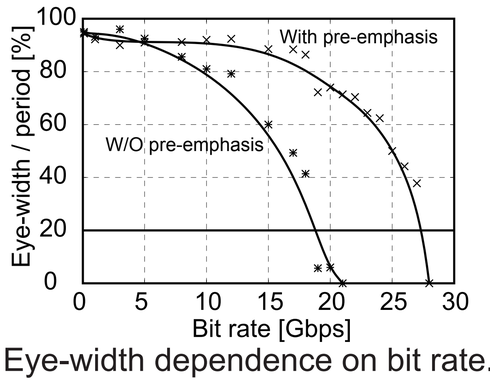
Dependence on delay τ.



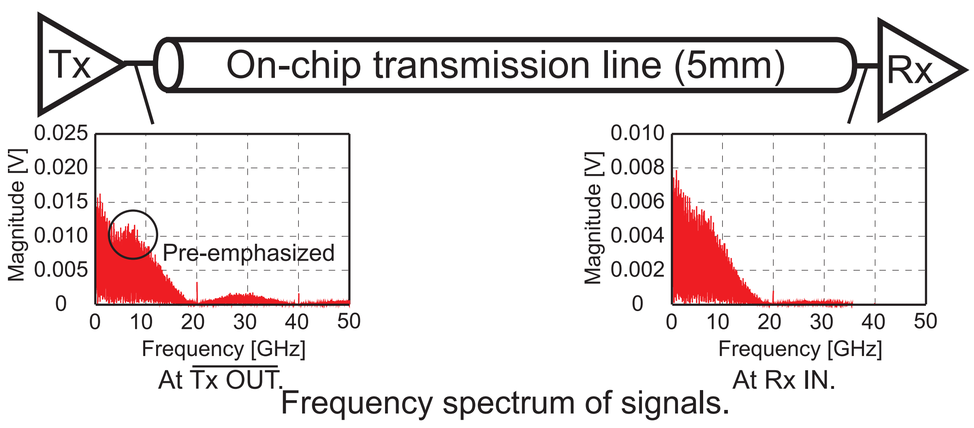
Dependence on emphasis amplitude.



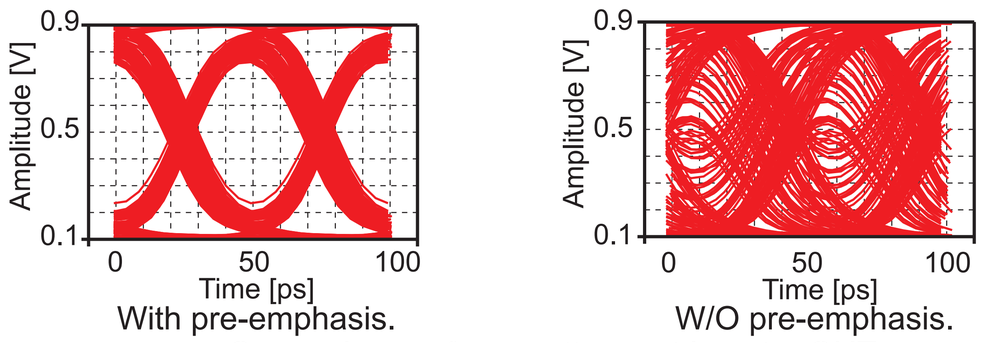
Input signal.



Eye-width dependence on bit rate.



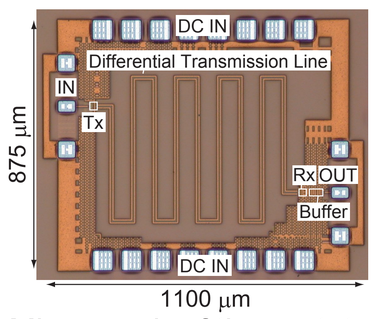
Frequency spectrum of signals.



Comparisons of eye-patterns at Inverter OUT.

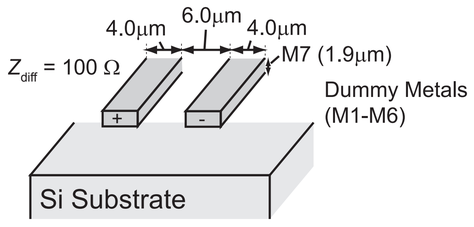
Experimental Results

Fabricated in 90nm Si CMOS



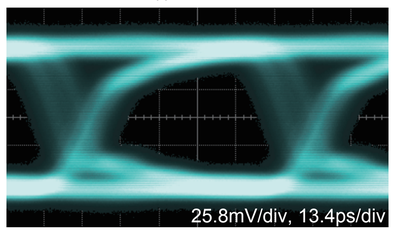
Micrograph of the prototype.

Area of Tx: 45×20μm²
Rx: 30×18μm²

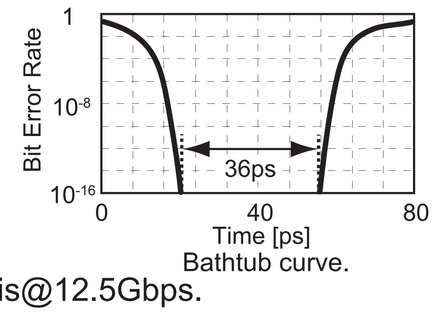


Cross section of the on-chip differential transmission line. The line length is 5 mm.

Input voltage: 1.0V_{pp}, PRBS from pulse pattern generator (max 12.5Gbps): 2^{11}-1

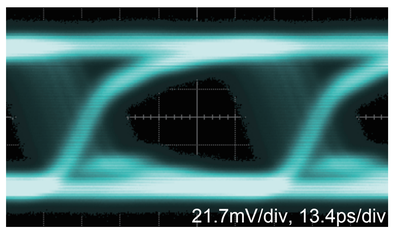


Eye-pattern.

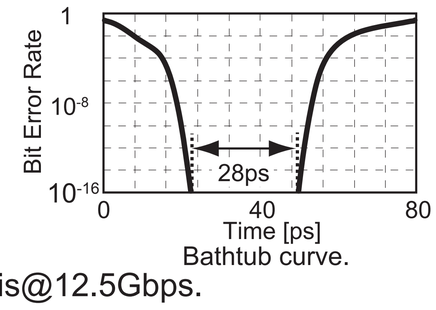


Bathtub curve.

With pre-emphasis@12.5Gbps.



Eye-pattern.



Bathtub curve.

W/O pre-emphasis@12.5Gbps.

Better signal transmission is achieved by pre-emphasis.

Summary

- A pre-emphasis Tx is proposed.
  Small circuit area and low power
- The validity was confirmed by the evaluating test chip.

Performance

Technology	90 nm COMS
Supply voltage	1.0 V
Power consumption*	6.9 mW@12.5 Gbps
Bit rate*	Over 12.5 Gbps
Energy per bit*	0.55 pJ/bit@12.5 Gbps
Circuit area	Tx: 45×20 μm² Rx: 30×18 μm²

*Measurement data