An Over-12-Gbps On-Chip Transmission Line Interconnect with a Pre-Emphasis Technique in 90 nm CMOS

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Background

High-performance LSI
Multiple circuit block configuration
On-chip interconnects among circuit blocks
Parallel interconnection → Serial interconnection
Key issues: Wideband, low latency and low power consumption

Pre-emphasis Technique

Signal quality is degraded at high-frequency because of the skin effect.

Compensation techniques for frequency dependence of transmission line loss

Tx side: Pre-emphasis
Rx side: Equalization

Rising and falling edges of Tx output are pre-emphasized.

Design

Input signal: 1.0Vpp, PRBS; 2¹-1, 20Gbps

Purpose

High-speed on-chip signaling

• Differential transmission line
• Pre-emphasis transmitter circuit

Small circuit area and low power operation

Circuit Operation

Pre-emphasis transmitter circuit
Differential transmission line

State 1 (t<) IN is High, Tx OUT is Low.
State 2 (t<2<) IN is Low, Tx OUT is High.
State 3 (t<2<) IN' is High (M3:ON, M5:OFF).
The rising edge is emphasized.
State 4 (t<2<) IN' is High, Tx OUT is Low.
State 5 (t<2<) IN' is Low (M3:ON, M5:OFF).
The falling edge is emphasized.

Experimental Results

Fabricated in 90nm Si CMOS

Cross section of the on-chip differential transmission line. The line length is 5 mm.

Better signal transmission is achieved by pre-emphasis.

Summary

• A pre-emphasis Tx is proposed.
  Small circuit area and low power
• The validity was confirmed by the evaluating test chip.

Performance

<table>
<thead>
<tr>
<th>Technology</th>
<th>90 nm CMOS</th>
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</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.0 V</td>
</tr>
<tr>
<td>Power consumption*</td>
<td>6.9 mW/12.5 Gbps</td>
</tr>
<tr>
<td>Bit rate*</td>
<td>Over 12.5 Gbps</td>
</tr>
<tr>
<td>Energy per bit*</td>
<td>0.55 pJ/bit/12.5 Gbps</td>
</tr>
<tr>
<td>Circuit area</td>
<td>Tx: 45×20 µm², Rx: 30×18 µm²</td>
</tr>
</tbody>
</table>

*Measurement data