ACCURATE PARASITIC INDUCTANCE DETERMINATION OF A CERAMIC CAPACITOR THROUGH 2-PORT MEASUREMENT

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Background

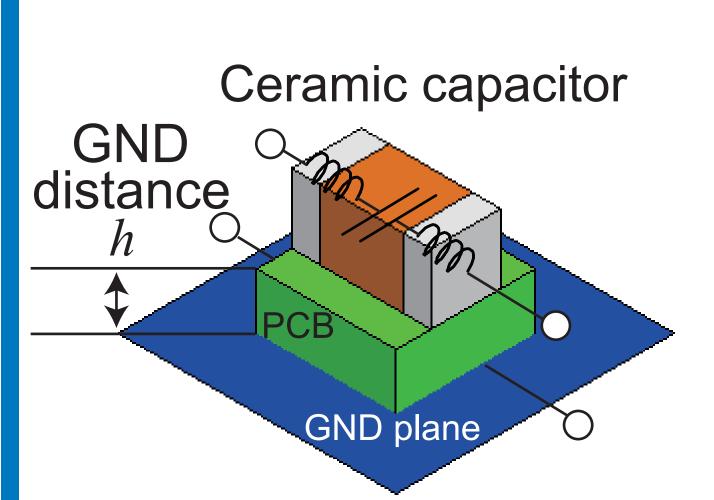
Electrical device trends

- High frequency operation
- Low operation voltage
- High power consumption

Voltage fluctuation and EMI problems become severe

Simulation of Print Circuit Board (PCB) is important

Purpose of this work

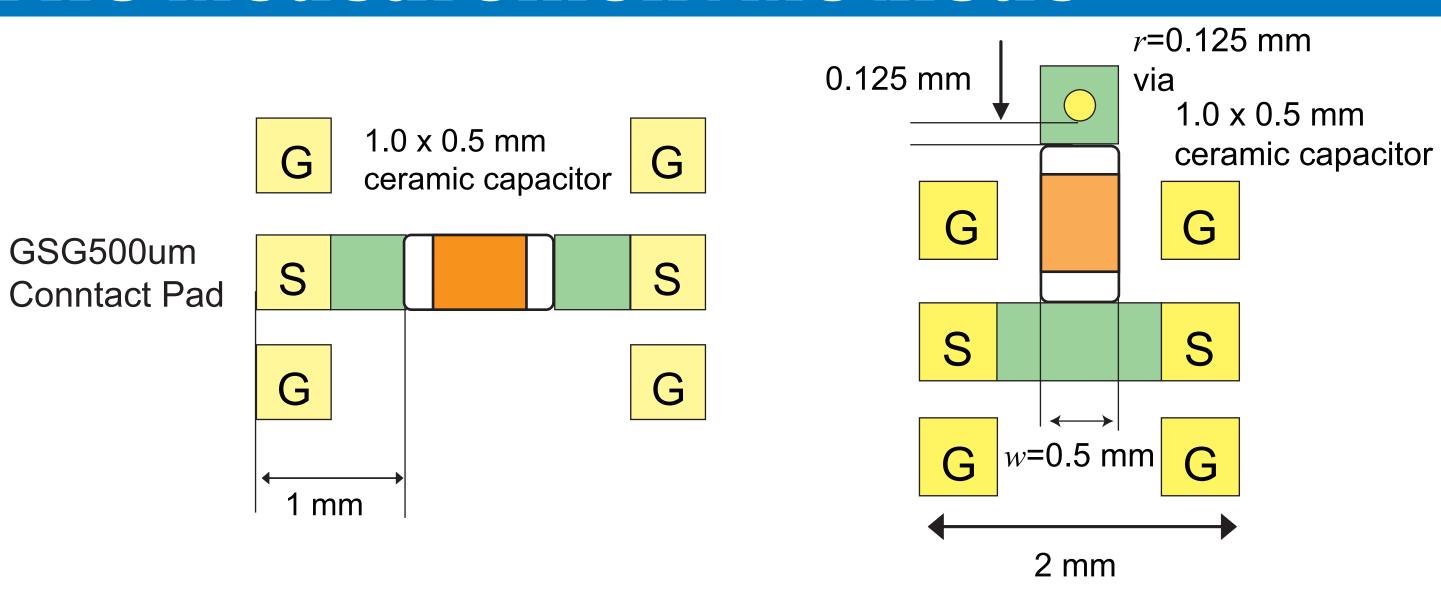


Our 2-port ceramic capacitor model

- Parasitic L of ceramic capacitor is too low (in the order of 100pH)
- ullet Parasitic L is an open-loop partial L (Both ends of the model are opened)
- lacksquare Parasitic L depends on GND distance h

We propose accurate determination method of parasitic \boldsymbol{L} of capacitor and validate proposed model

Two Measurement Methods



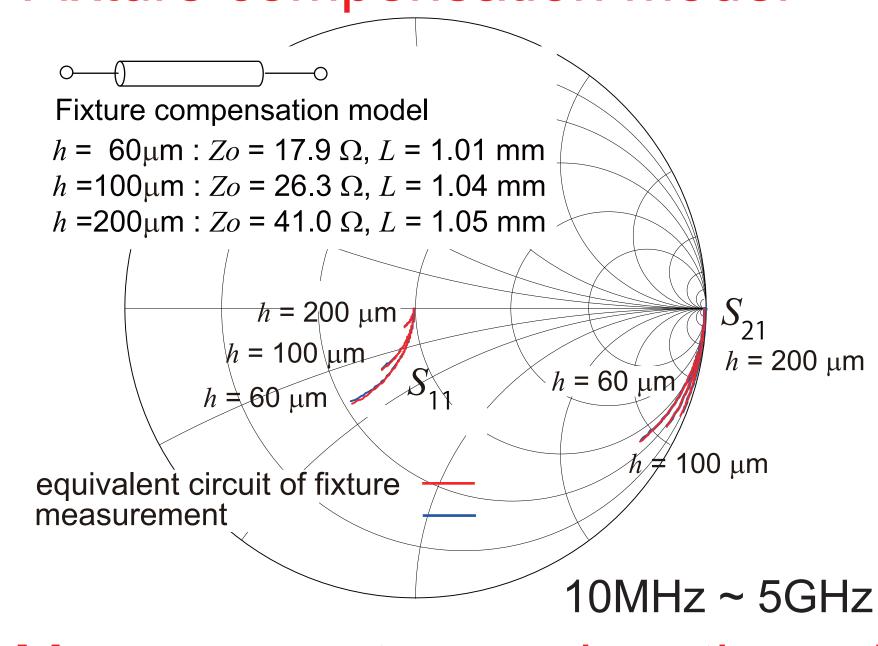
GND distance $h=60~\mu m$, 100 μm , and 200 μm .

- (a) Series 2-port meas.
- (b) Shunt 2-port meas.

Required compensation

- Series: phase rotation by access lines
- Shunt: via and access line L for open loop L

Fixture compensation model



Measure through pattern for compensation model

Symmetric equivalent circuit model of the through pattern is constructed

Measurement procedure through series fixture

 $\mathbf{S}_{\mathrm{meas}}$: Measured S parameter of capacitor with fixture

 S_{fix} : S parameter of the fixture model

$$\mathbf{T}_{\text{cap}} = \mathbf{T}_{\text{fix}}^{-1} \mathbf{T}_{\text{meas}} \mathbf{T}_{\text{fix}}^{-1}$$

$$Z_{\text{cap}} = \frac{1 - S_{\text{cap}} 21 - S_{\text{cap}} 12 - |\mathbf{S}_{\text{cap}}|}{1 - S_{\text{cap}} 11 - S_{\text{cap}} 22 - |\mathbf{S}_{\text{cap}}|}$$

$$L_{\text{cap}} = \frac{\text{Im}\{Z_{\text{cap}}\}}{\langle U_{\text{cap}} \rangle}$$

Measurement procedure through shunt fixture

 $\mathbf{S}_{\mathrm{meas}}$: Measured S parameter of capacitor with fixture

 $\mathbf{S}_{\mathrm{fix}}$: S parameter of the fixture model

 $L_{
m excess}$: Excess via and pattern L (see proceeding paper for detail)

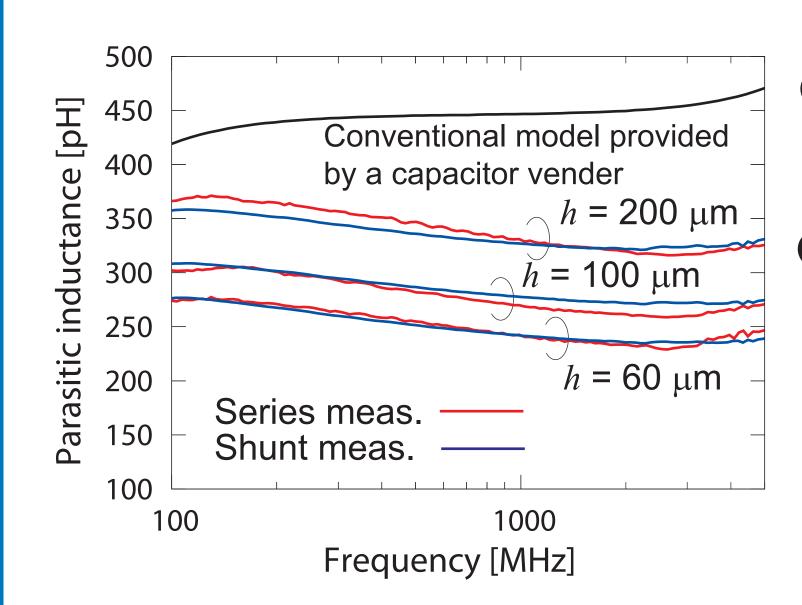
$$\mathbf{T}_{\text{cap}} = \mathbf{T}_{\text{fix}}^{-1} \mathbf{T}_{\text{meas}} \mathbf{T}_{\text{fix}}^{-1}$$

$$Z_{\text{cap}} = 25 \frac{S_{\text{cap}} 21}{1 - S_{\text{cap}} 21}$$

$$L_{\text{cap}} = \frac{\text{Im}\{Z_{\text{cap}}\}}{\omega} - L_{\text{excess}}$$

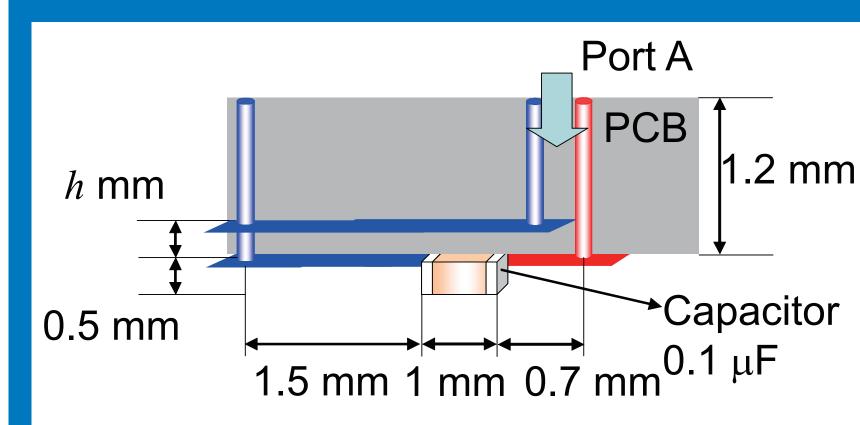
Parasitic L through Measurement

Measurement result of 1.0x0.5mm ceramic capacitor



- Both measurement match very well
- Parasitic L takes different value by more than 100 pH depending on the GND distance h.

Validation of proposed model



A PDN inductance from Port A is simulated by using proposed model and compared with measurement result.

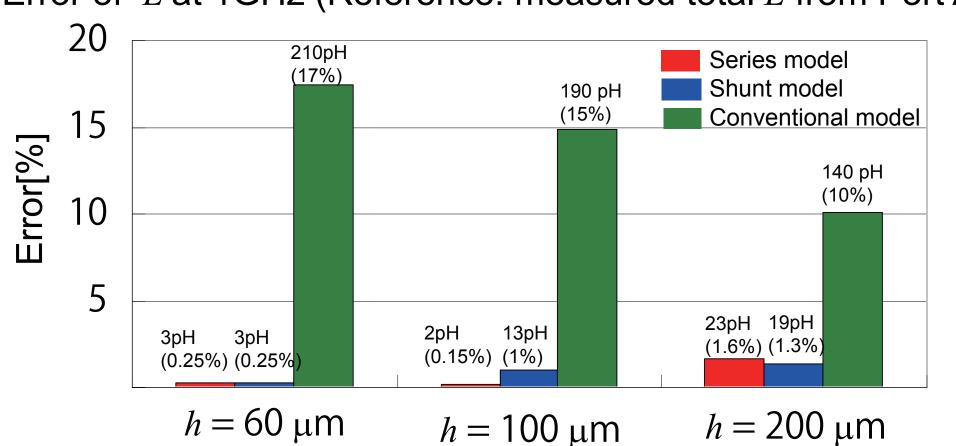
Dimension of the PDN of PCB(cross sectional view)

Simulation procedure

- 1) Calculate 3-port PCB model by using electromagnetic simulator
- 2) Extract 2-port capacitor model by the measurements.
- 3) Connect the capacitor model into the 3-port PCB model and then calculate total inductance from port A.

Simulation and measurement result

Error of L at 1GHz (Reference: measured total L from Port A)



Sim. results by using proposed model match very well with meas.

Conclusions

- Two accurate 2-port measument methos of parasitic L
 for ceramic capacitor are proposed
- Parasitic L measured by two different methods matches well
- Our proposed 2-port model is useful for accurate PDN simulation.