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Design of CMOS inverter-based output buffers adapting the Cherry-Hooper broadbanding technique

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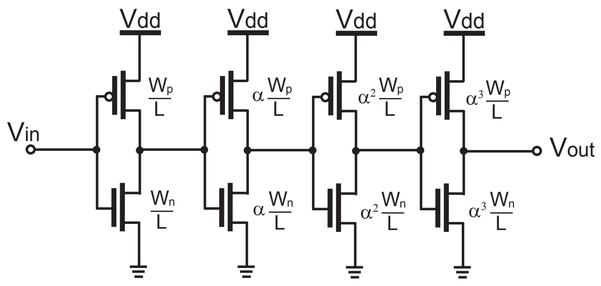
Background&Purpose

- On-chip Output Buffers
  - send off the output data of a digital integrated circuit
  - drive large capacitive loads/low-resistance loads(typically 50Ω)
  - invariably affect measurement results
    - Exponential horn topology



minor modifications

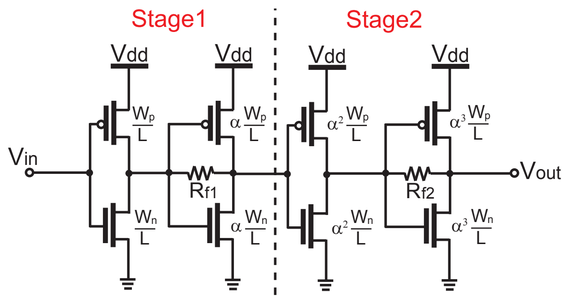
wide bandwidth

large jitter due to a very high gain

Requirements : wide bandwidth, low gain, low jitter, high drivabilty

Purpose

Establishment of a methodology for designing CMOS inverter-based output buffers considering these requirements

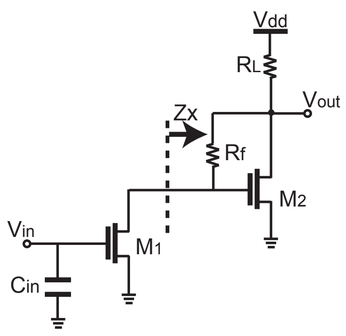


wide bandwidth

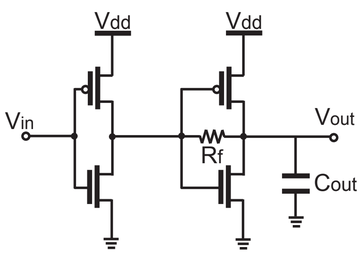
low jitter

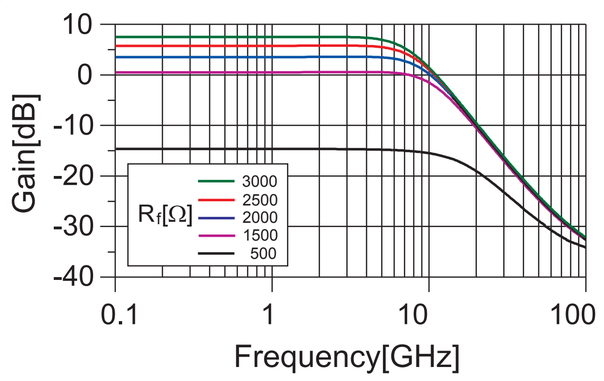
Cherry-Hooper Broadbanding Technique

NMOS implementation of the Cherry-Hooper amplifier.



CMOS Cherry-Hooper amplifier.





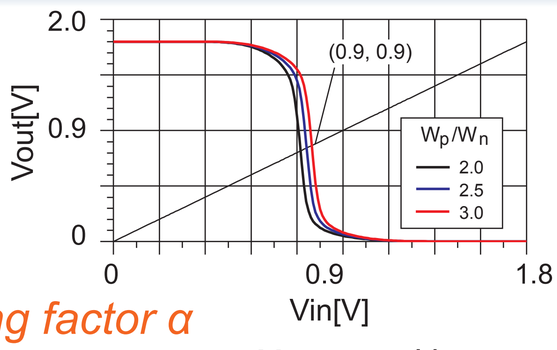
Cutoff frequency of the Cherry-Hooper amplifier does not depend significantly on Rf

A design procedure(180 nm Process)

A. Choose Wp/Wn ratio

Jitter reduction

- Wp/Wn value that brings the inverter switching threshold close to Vdd/2 should be chosen.
- Wp/Wn =3 was chosen in this design.



B. Determine gate widths and scaling factor α

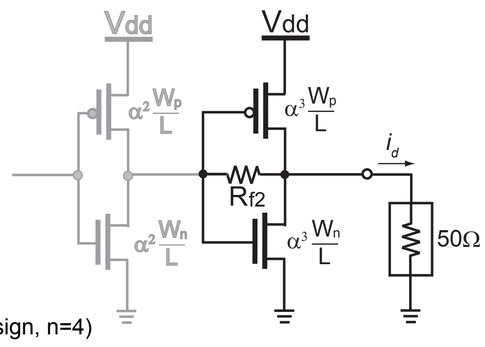
The rightmost inverter

- should drive a 50 Ω load and produce a certain voltage
  - NMOS gate widths can be found from transient simulation including a feedback resistor R_{f2}.
  - The initial choice of R_{f2} has only a minor impact on *id.*

Scaling factor α

$$\alpha = \left(\frac{\text{NMOS width of the rightmost inverter}}{\text{NMOS width of the leftmost inverter}}\right)^{\frac{1}{n}}$$

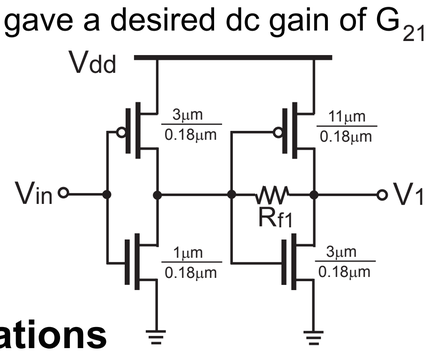
n:stage # (in this design, n=4)

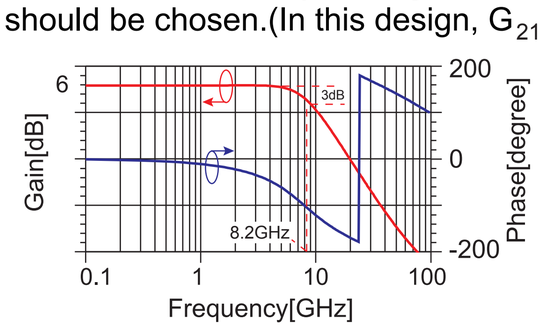


C. Determine feedback resistances R_{f1} and R_{f2}

The first CMOS Cherry-Hooper stage

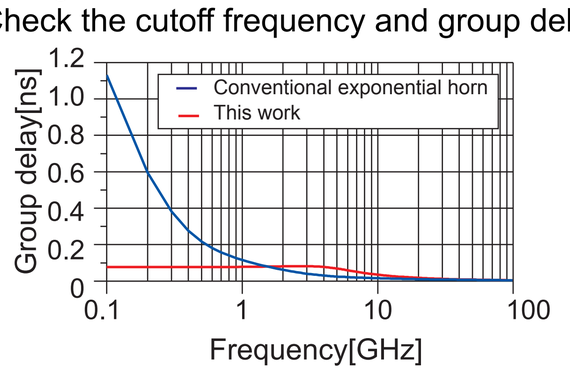
- All parameters other than the feedback resistance R_{f1} have already been given.
  - Rf1 value that gave a desired dc gain of G_{21} should be chosen.(In this design, G_{21} = 6dB.)

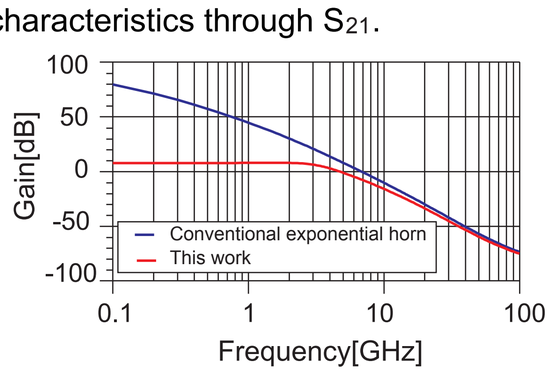




Final simulations

- Put in all the parameter values determined so far and perform transient simulations.
  - Check the output signal swing and adjust the value of R_{f2} so that the desired voltage swing is achieved.
- Check the cutoff frequency and group delay characteristics through S_{21}.

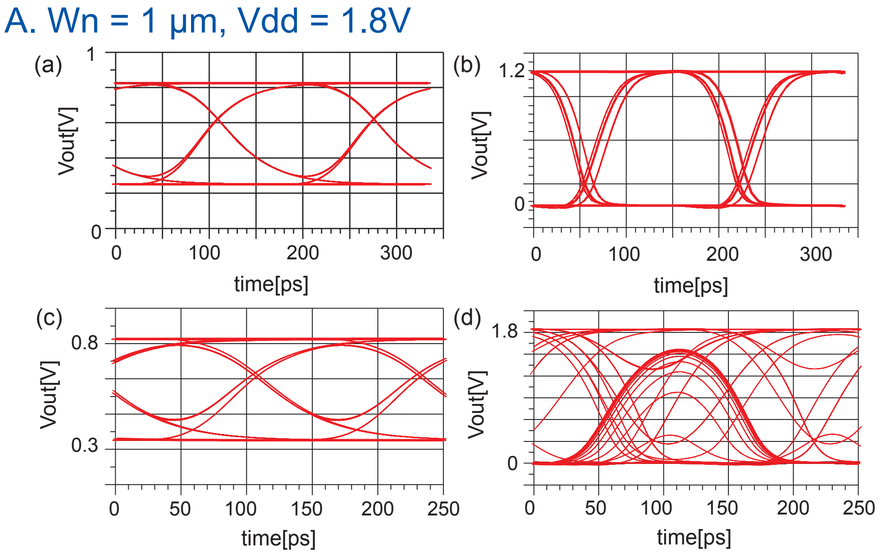




Simulation Results

Performance comparison between the proposed buffers and that without the feedback resistors for a few scenarios.

A. Wn = 1 μm, Vdd = 1.8V

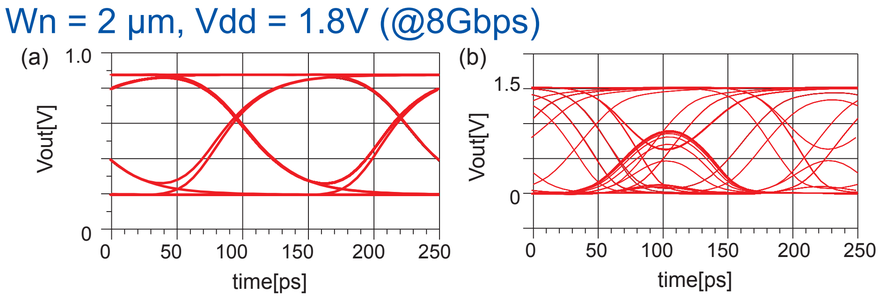


@7Gbps

The proposed buffer conventional @8Gbps

Both buffers are functioning but the proposed buffer exhibits less jitter.
The proposed buffer can operate at higher bit-rate.

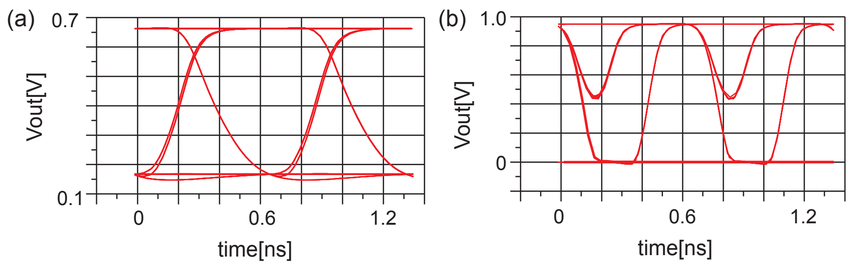
B. Wn = 2 μm, Vdd = 1.8V (@8Gbps)



The proposed buffer conventional

The proposed buffer shows superior performance even if the gate width is changed.

C. Wn = 1 μm, Vdd = 1.2V



The proposed buffer conventional

The proposed buffer is promising for low voltage use.

Conclusion

- A methodology for designing CMOS inverter-based output buffers apapting Cherry-Hooper amplifier considering speed, gain, jitter, and drivability requirements is proposed.
- The validity of the procedure was confirmed in different scenarios by simulation.
- The proposed buffer is expected to offer higher speed than a commonly used chain of inverters with exponentially increasing size.

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