High-Speed and Low-Power On-Chip Transmission Line Interconnect Technologies

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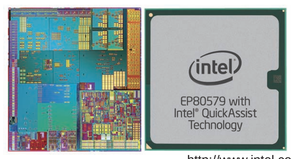
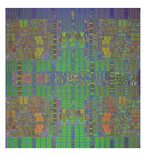
Introduction

Miniaturization of Si CMOS technologies

- System-on-a-chip(SoC) has become possible



http://www.intel.co.jp/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Interconnects among circuit blocks

- greatly affect whole chip capabilities
- wide-bandwidth, low-latency and low-power are required

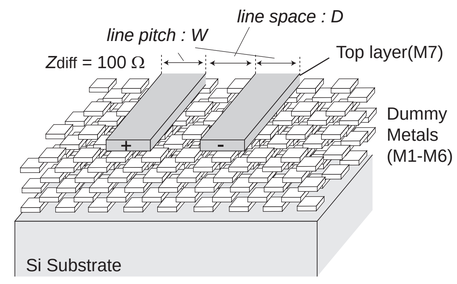
Conventional RC line : repeater insertion

On-chip Transmission Line Interconnects(TLIs)

- have better characteristics : bandwidth, latency, latency

The best to use for interconnects in LSIs

Three prototypes of on-chip TLIs are introduced



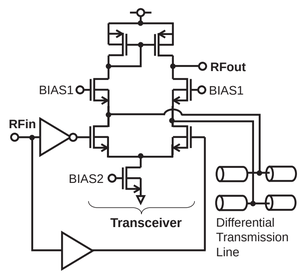
The metal of line : Aluminum

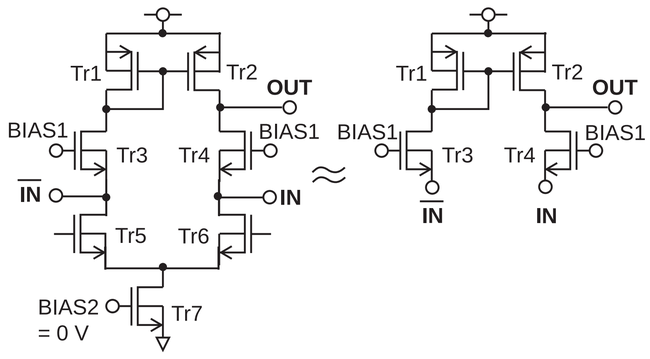
Dielectric : Silicon dioxide

8Gbps Multi-Drop/Bidirectional of On-Chip TLIs

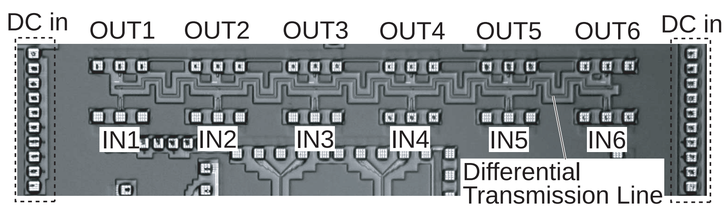
Two-way transceiver

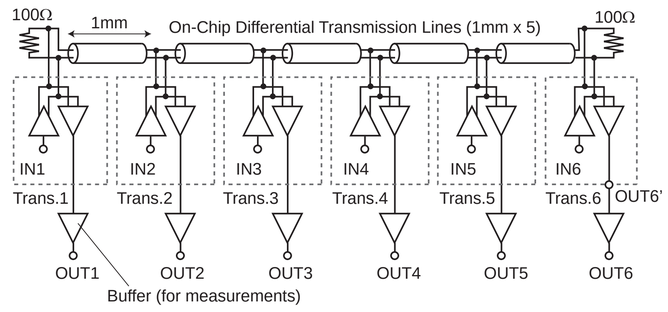
- can serve as transceiver(Tx) and receiver(Rx)
- can save circuit area

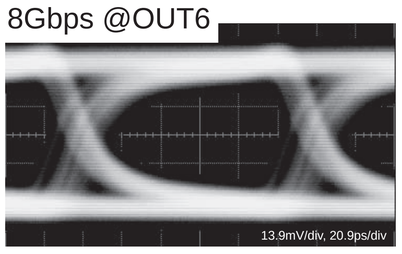


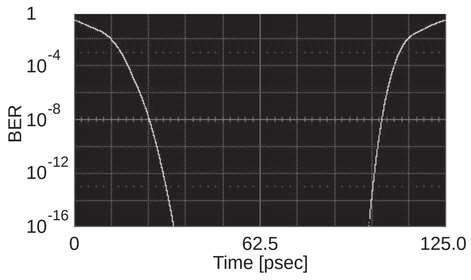


Tx mode Rx mode









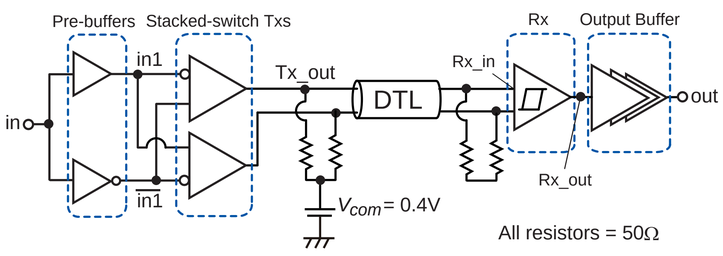
Technology: 90nm Si CMOS
Supply voltage: 1.0V
Power @8Gbps: 1.2mW/Trans.
Total power (Tx and six Rx): 7.2mW
Simulated delay: 150ps/5mm
The maximum bit rate: 8Gbps
Energy per bit: 0.90pJ/bit

● H. Ito *et al.*, IEEE Journal of Solid-State Circuits, Vol. 43, No. 4, pp. 1020-1029, April 2008.
● H. Ito *et al.*, IEEE Symposium on VLSI Circuits, pp. 136-137, June 2007.

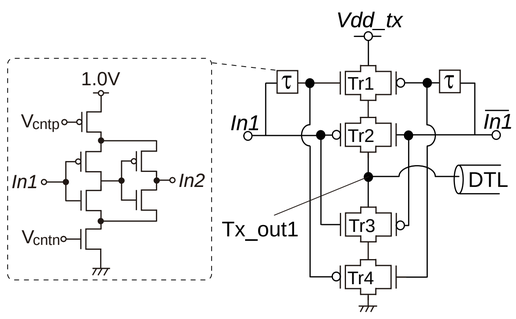
8Gbps 2.5mW On-Chip Pulsed-Current-Mode TLIs

Pulsed-Current-Mode signaling with a stacked-switch Tx

- mainly consists of transistors, which can save circuit area
- Pulse widths are adjustable

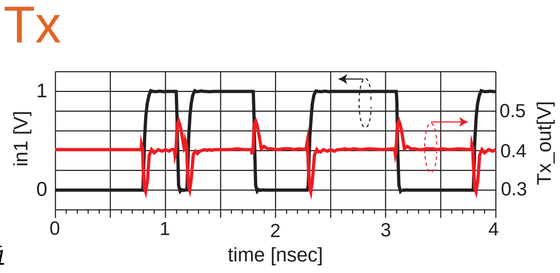


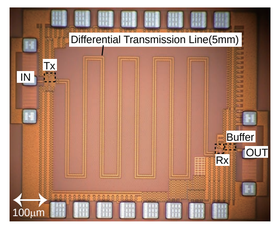
Schematic of PTLI*

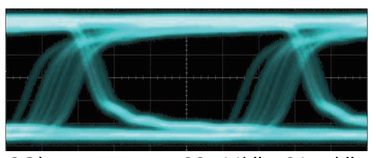


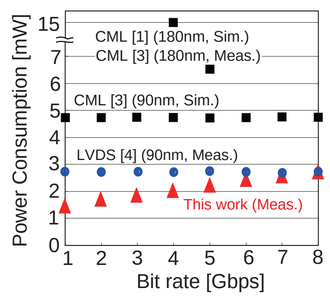
The stacked-switch Tx

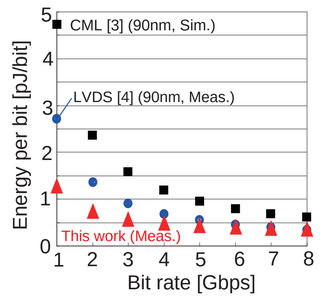
*:Pulsed-Current-Mode Transmission Line Interconnect
● T.Maekawa *et al.*, European Solid-State Circuits Conference, pp. 474-477, Sept. 2008..






8Gbps 38mV/div, 21ps/div





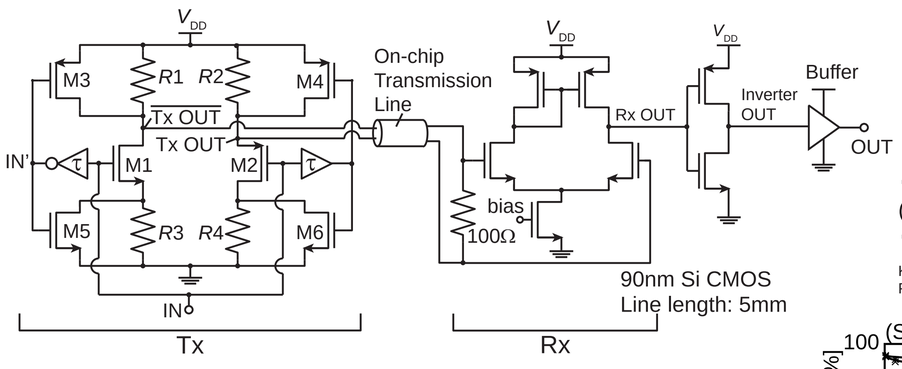
Process: 90nm Si CMOS
Supply Voltage : 1.0 V
Maximum bit rate: 8Gbps
Power consumption @8Gbps: 2.5mW
Energy per bit: 0.31pJ/bit
Delay (In-Rx_out, 5mm): 164ps

[1] S. Gomi *et al.*, IEEE Custom Integrated Circuits Conference, pp. 325-328, 2004. [3] T. Ishii *et al.*, IEEE Asian Solid-State Circuits Conference, pp. 131–134, 2006. [4] H. Ito *et al.*, IEEE International Interconnect Technology Conference, pp. 193-195, 2007.

Over-12Gbps on-chip TLI with pre-emphasis

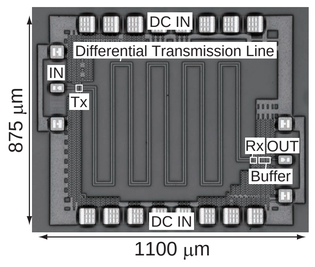
On-Chip Pre-emphasis Technique

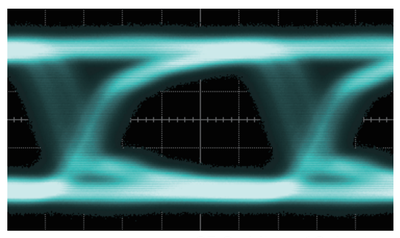
- transistors are used for performing equalization to save area
- compensating frequency dependences of loss to on-chip TLI

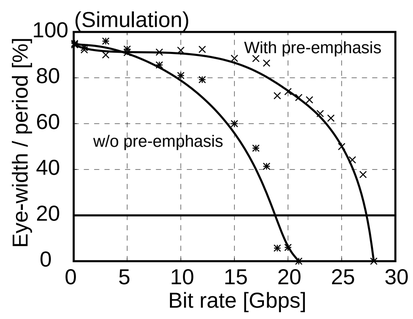


- Measured bit rate: 12.5Gbps (Maximum bit rate of PPG)
- Power consumption: 6.9mW

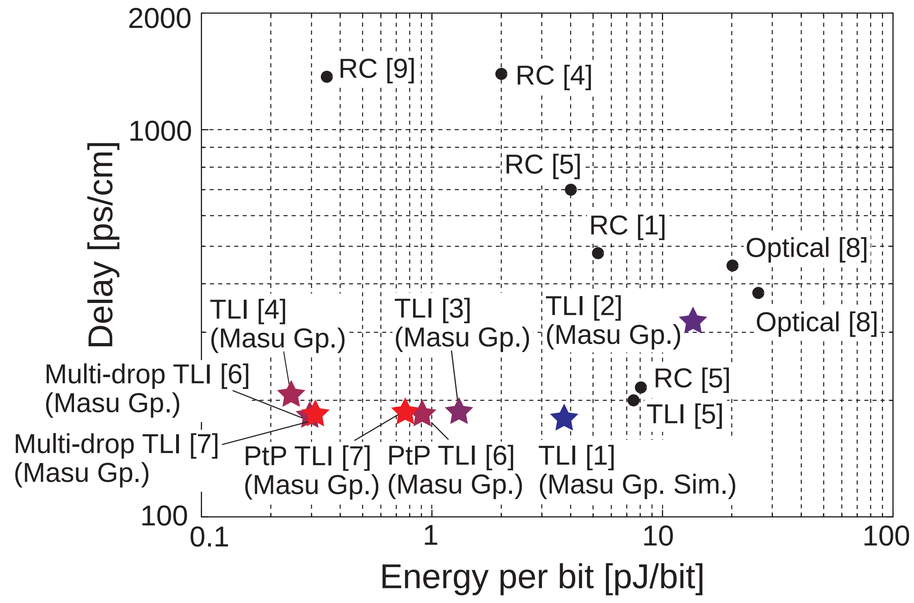
K. Miyashita *et al.*, 17th Conference on Electrical Performance of Electronic Packaging, Oct. 2008.




25.8mV/div, 13.4ps/div



Delay and Energy per bit of on-chip interconnects



[1] S. Gomi *et al.*, IEEE CICC, pp. 325-328, 2004.[2] H. Ito et al., IEEE A-SSCC, pp. 417-420, 2005
[3] T. Ishii *et al.*, IEEE A-SSCC, pp. 131–134, 2006.[4] H. Ito *et al.*, IEEE IITC, pp. 193-195, 2007.
[5] R. T. Chang *et al.*, IEEE JSSC, vol. 38, vo. 5, pp. 834-838, May, 2003.[6] H. Ito *et al.*, IEEE JSSC, vol. 43, no. 4. pp.1020-1029, April, 2008.
[7] T. Maekawa *et al.*, ESSCIRC, pp. 474-477, Sept. 2008. [8] E. D. Kyriakis-Bitzaros *et al.*, Journal of Lightwave Technology, vol.19, no. 10, pp. 1532-1542, Oct. 2001.[9] K. Lee *et al.*, IEEE ISSCC, pp.152-153, 2004.

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