

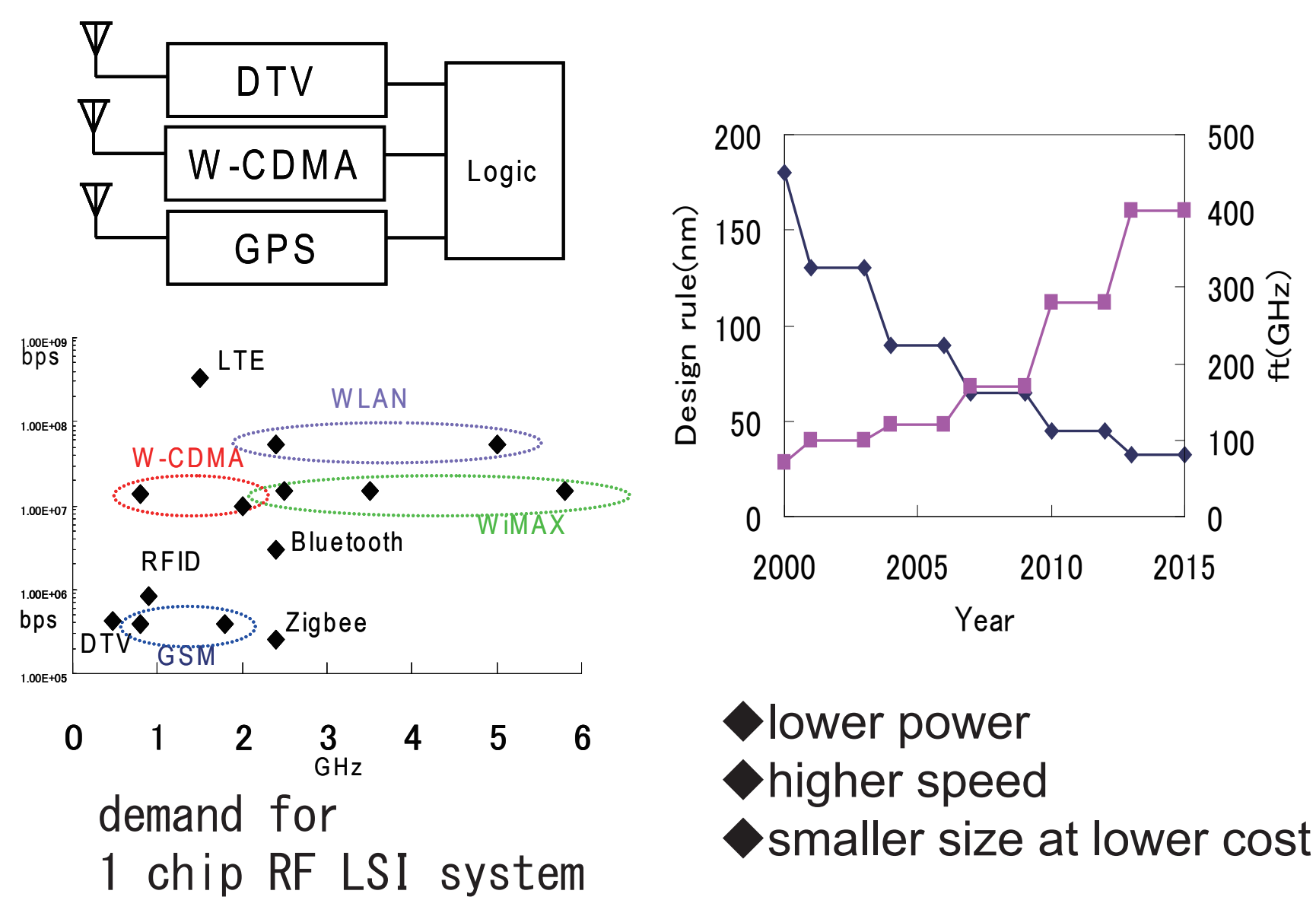
RF Signal Generator Based on Time-to-Analog Converter in 0.18 μm CMOS

Kazuo Nakano, Shuhei Amakawa, Noboru Ishihara, and Kazuya Masu

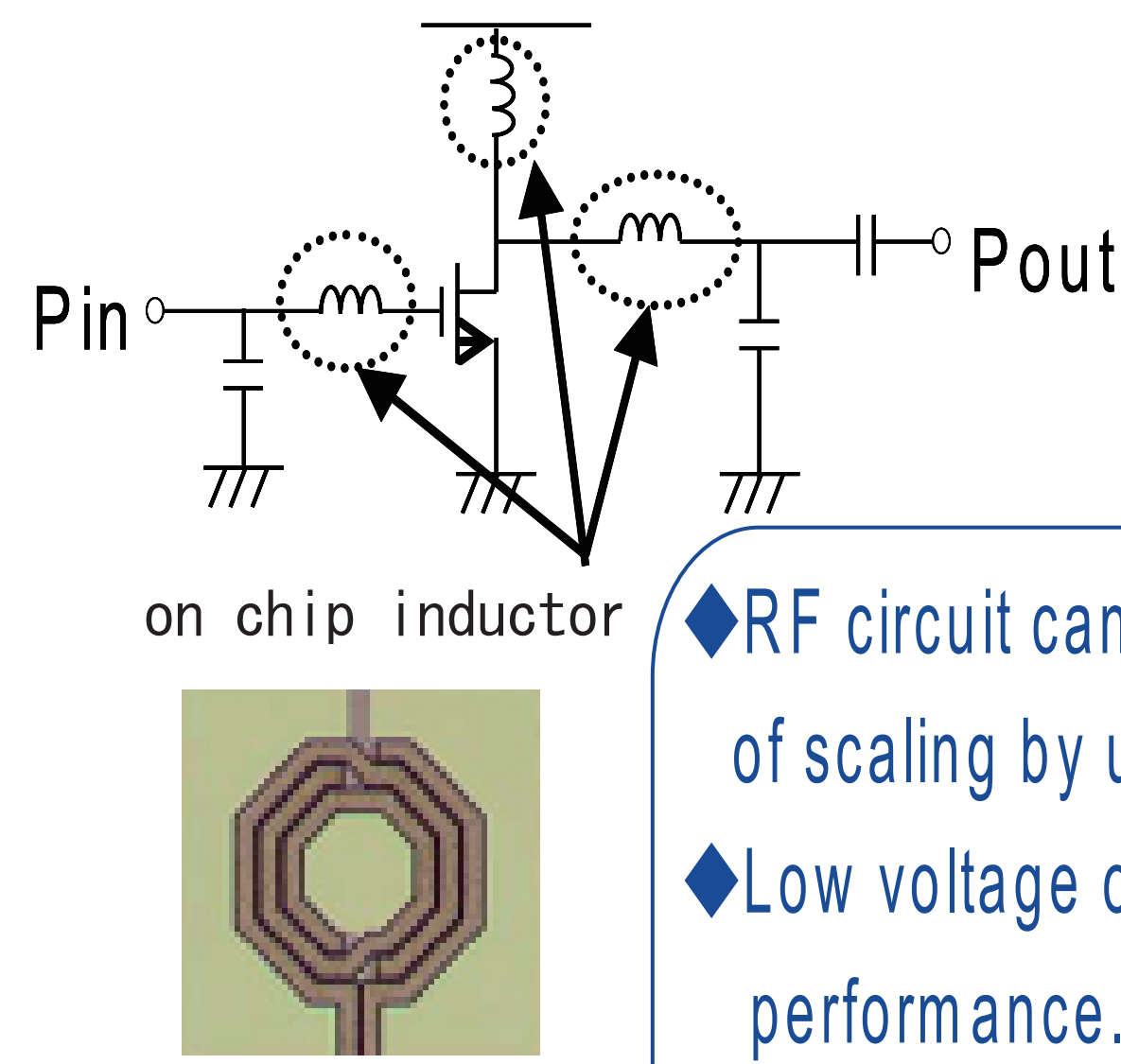
Integrated Research Institute, Tokyo Institute of Technology, Japan

1. Background

CMOS technology scaling



Si RF circuit

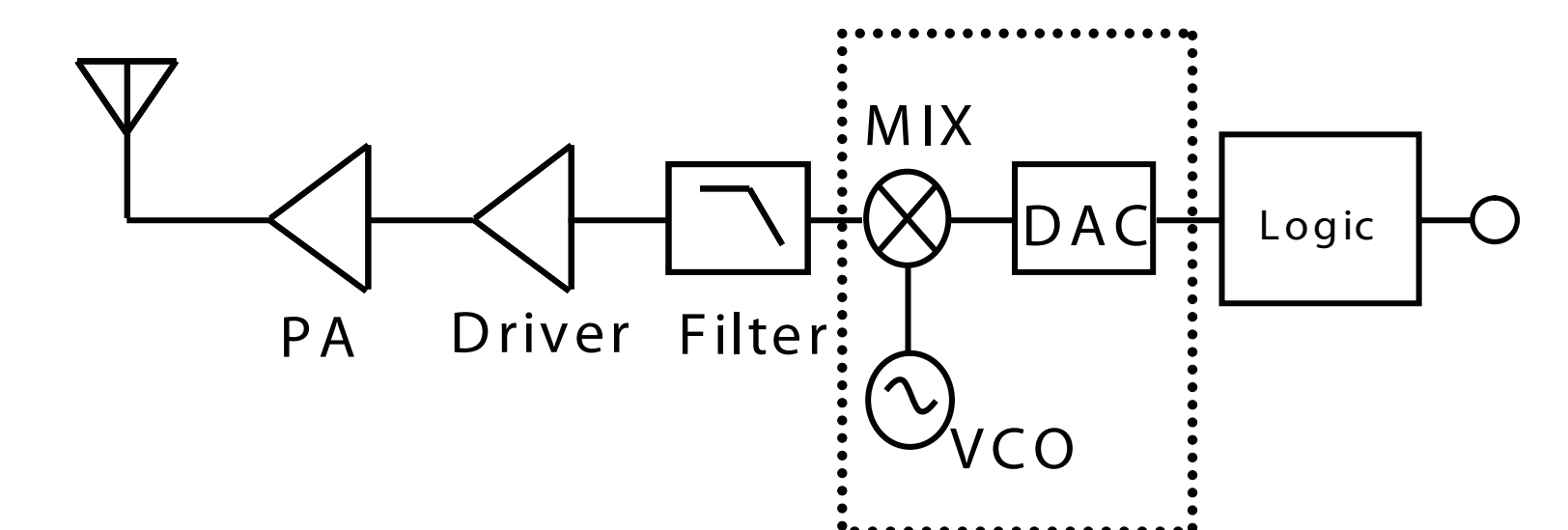


- ◆ RF circuit cannot make use of scaling by un-scalable device.
- ◆ Low voltage operation limits analog performance.

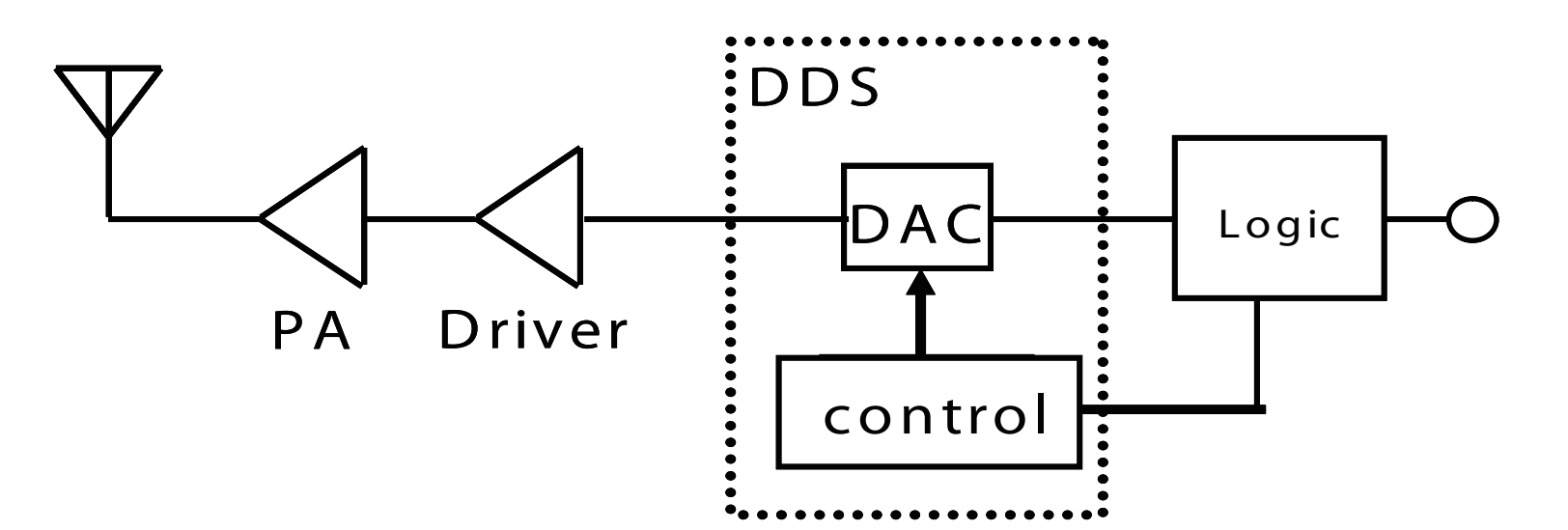
RF signal generator based on time-to-analog converter

Traditional RF Signal technology

Up conversion component used mixer



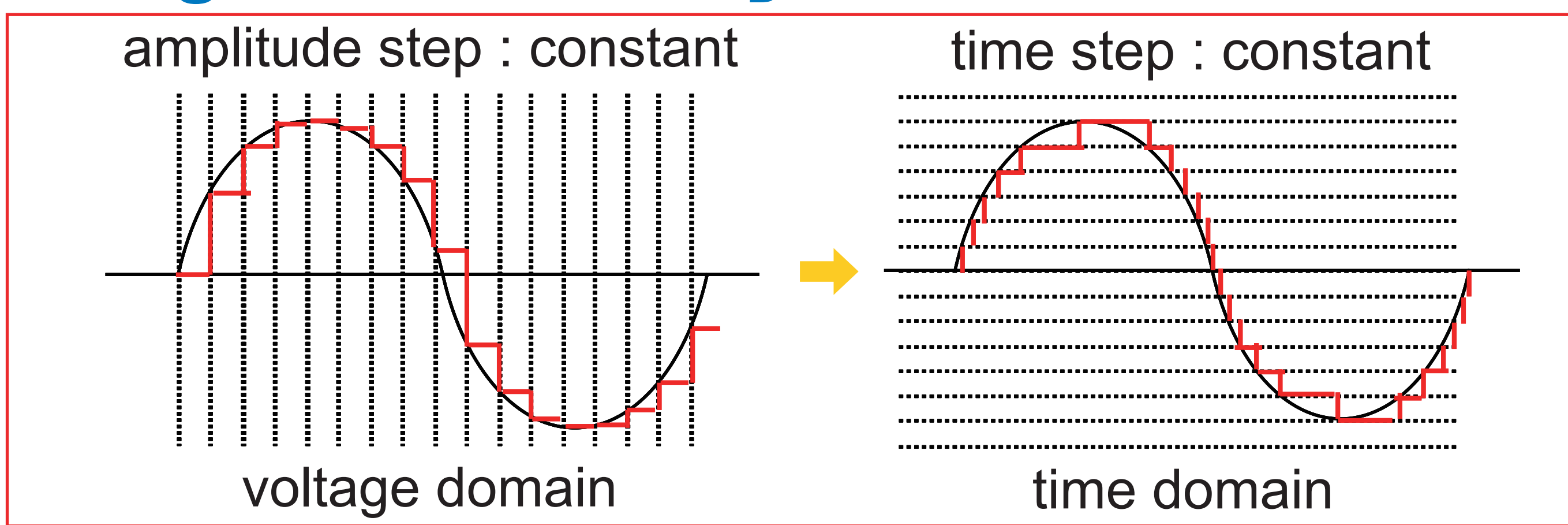
Direct digital synthesizer (DDS)



Lower voltage operation, associated with the CMOS technology scaling, limit the voltage domain resolution, enhancing the ordinary voltage domain DAC performances are not practical way.

2. Proposed RF Signal Generator

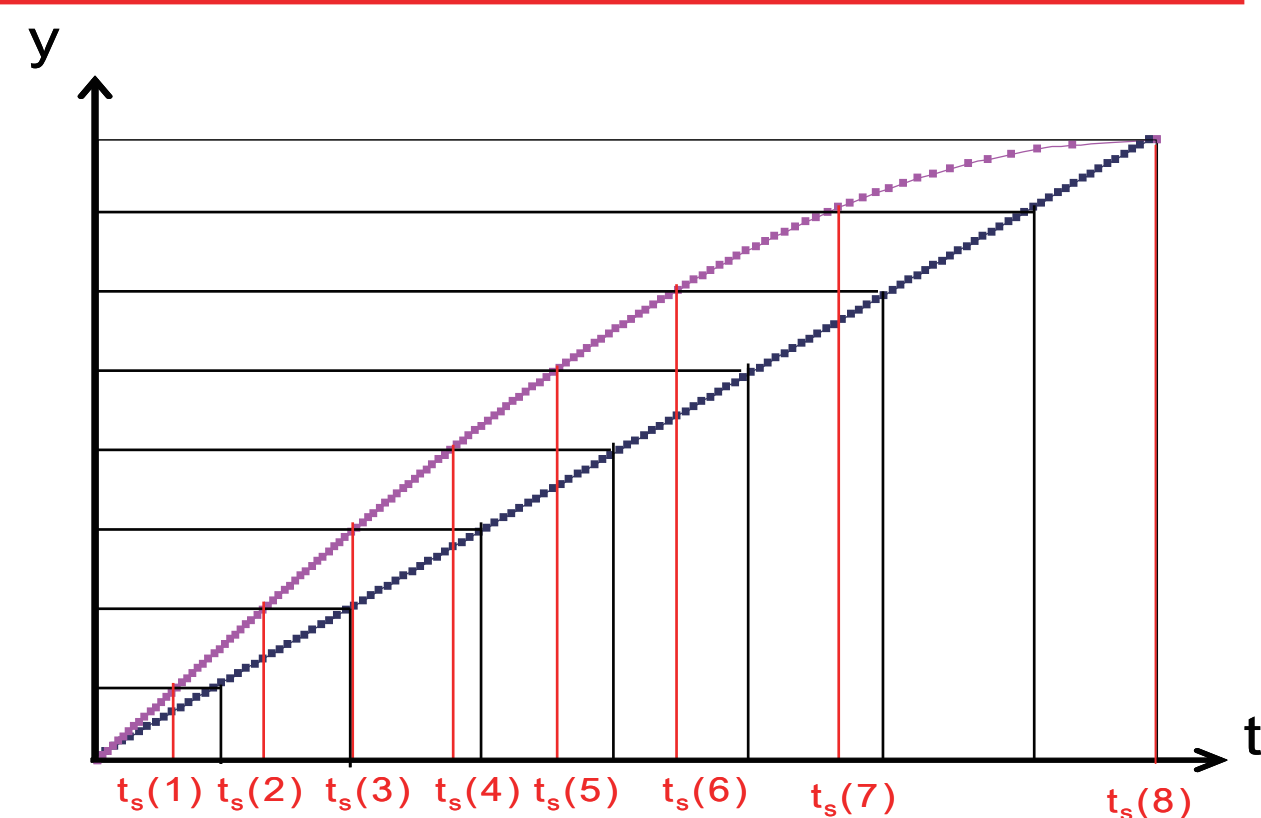
RF Signal Generator by time domain



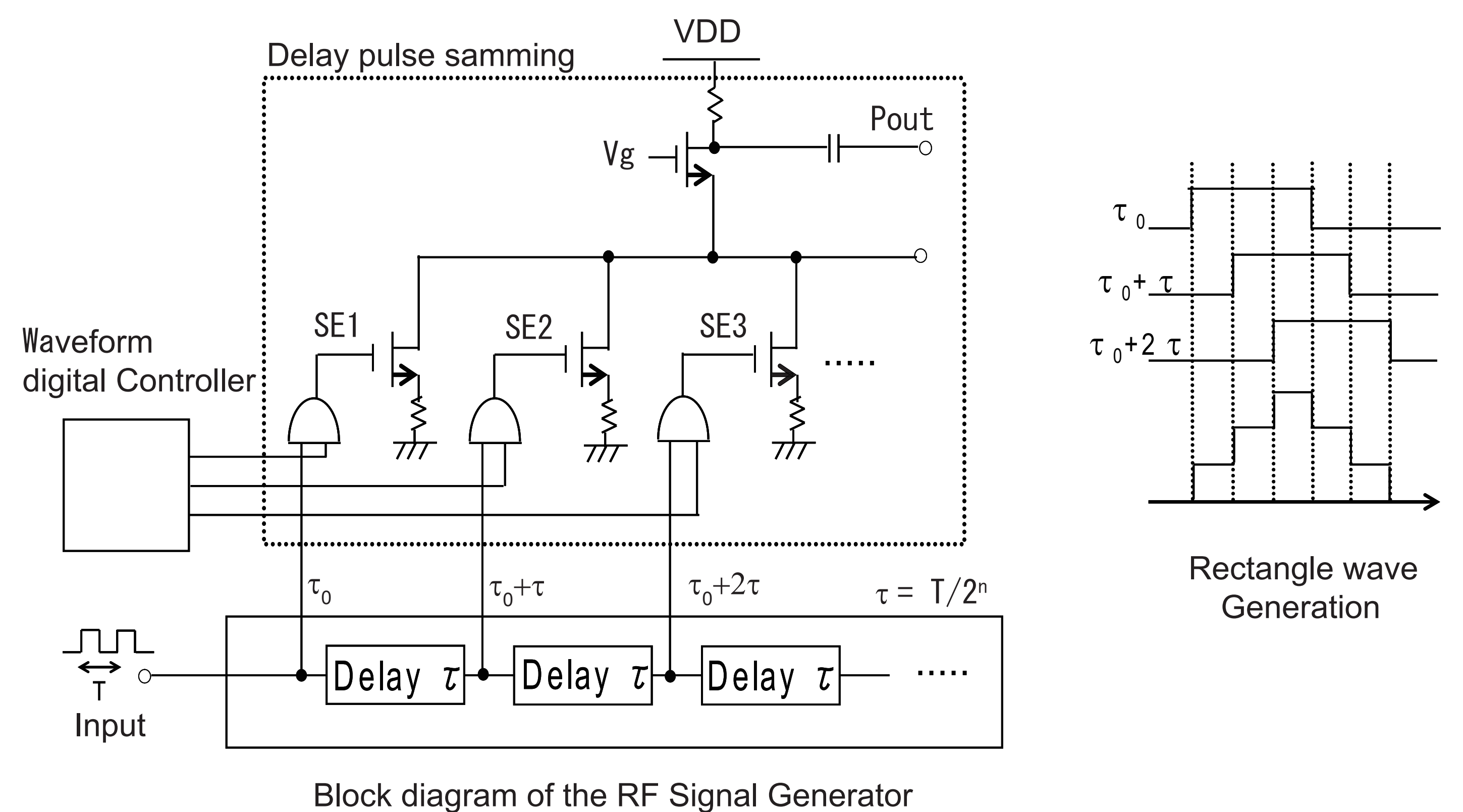
RF sin wave generation

$$y_s(n) = A \cdot \sin(2\pi f \cdot t_s(n))$$

$$\rightarrow t_s(n) = \left[\sin^{-1} \left(\frac{y_s(n)}{A} \right) \right] \cdot \frac{1}{2\pi f}$$

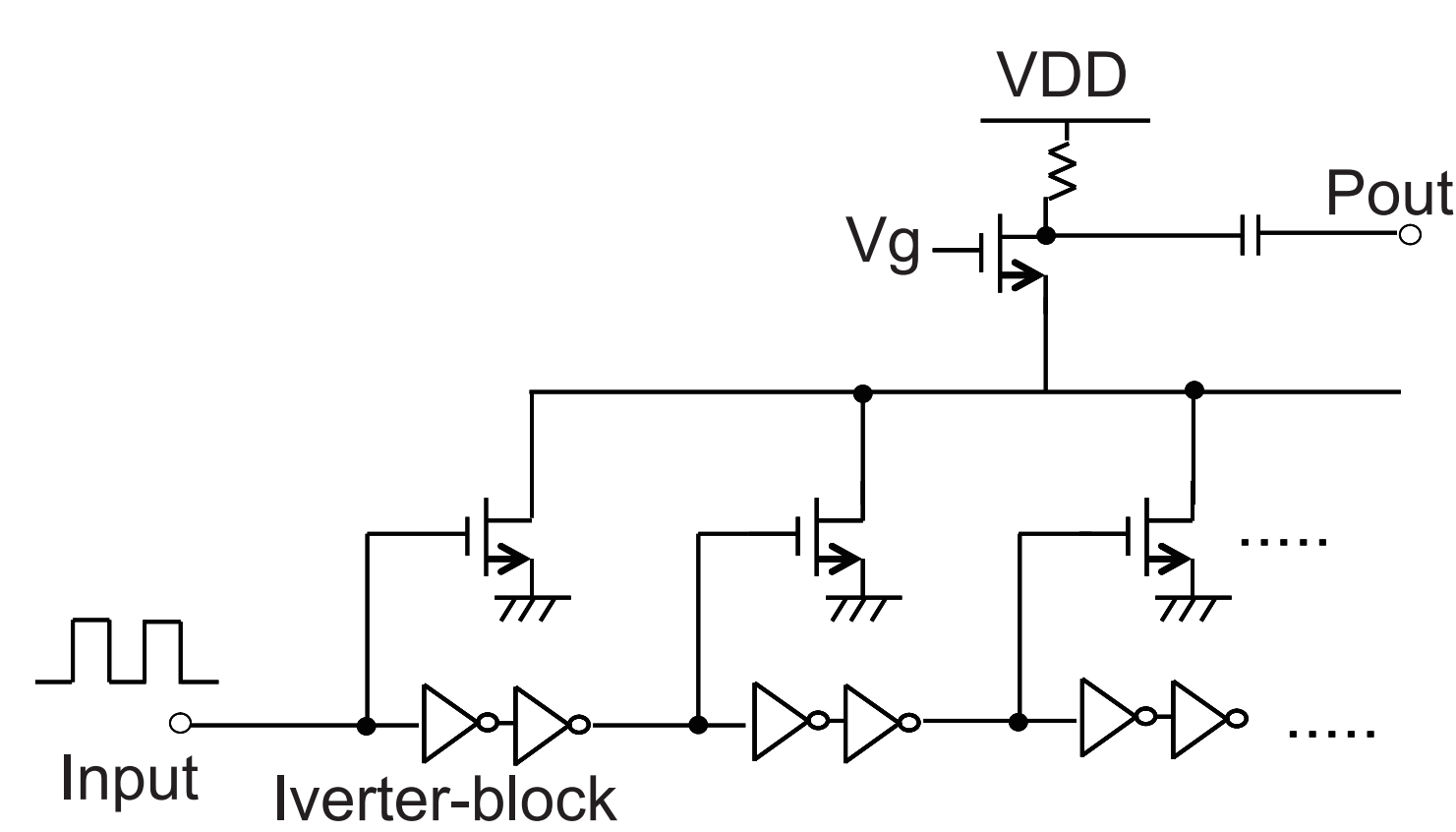


Block diagram of the RF Signal Generator



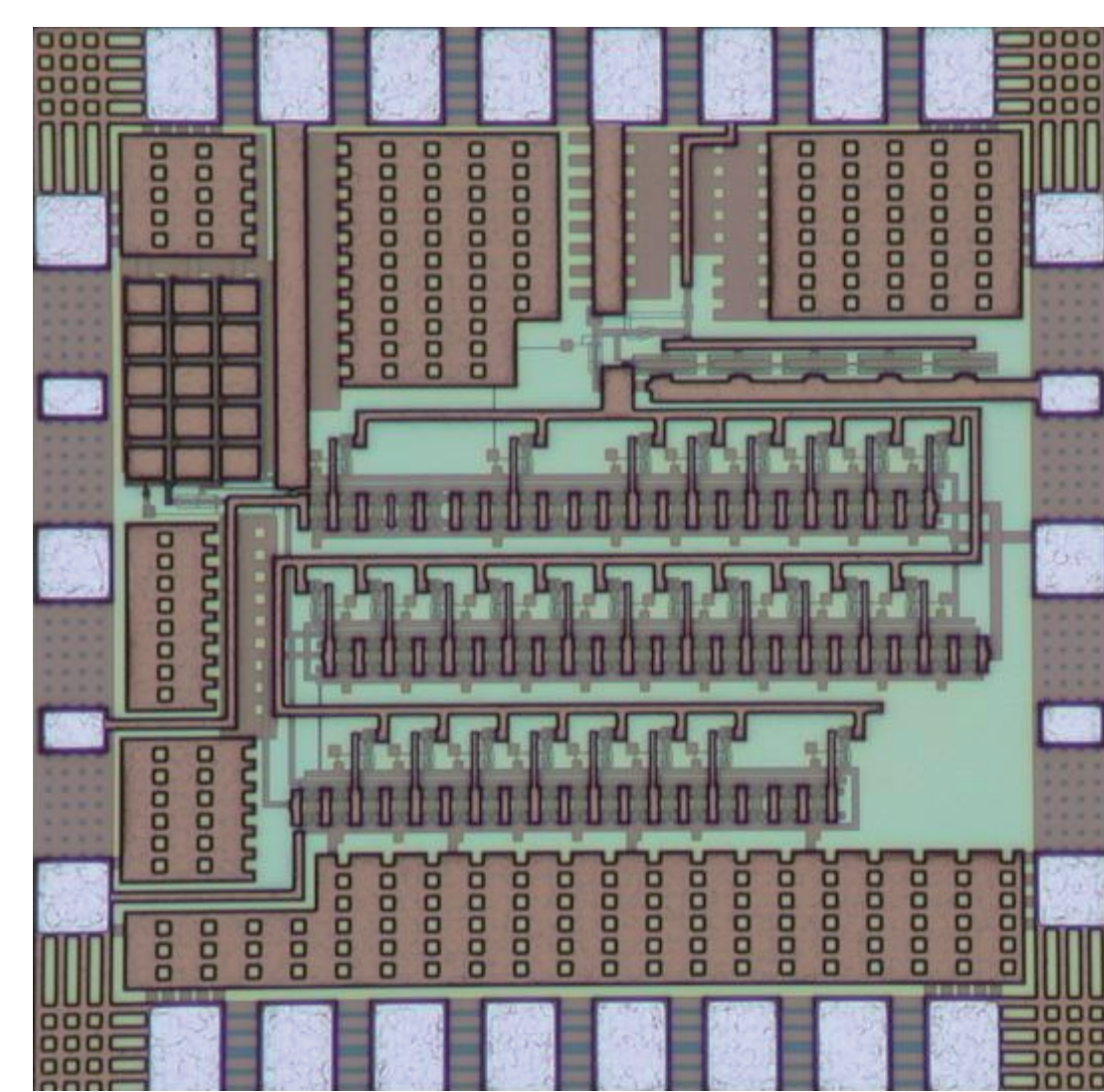
3. Measured Results

Test chip design of RF signal generator



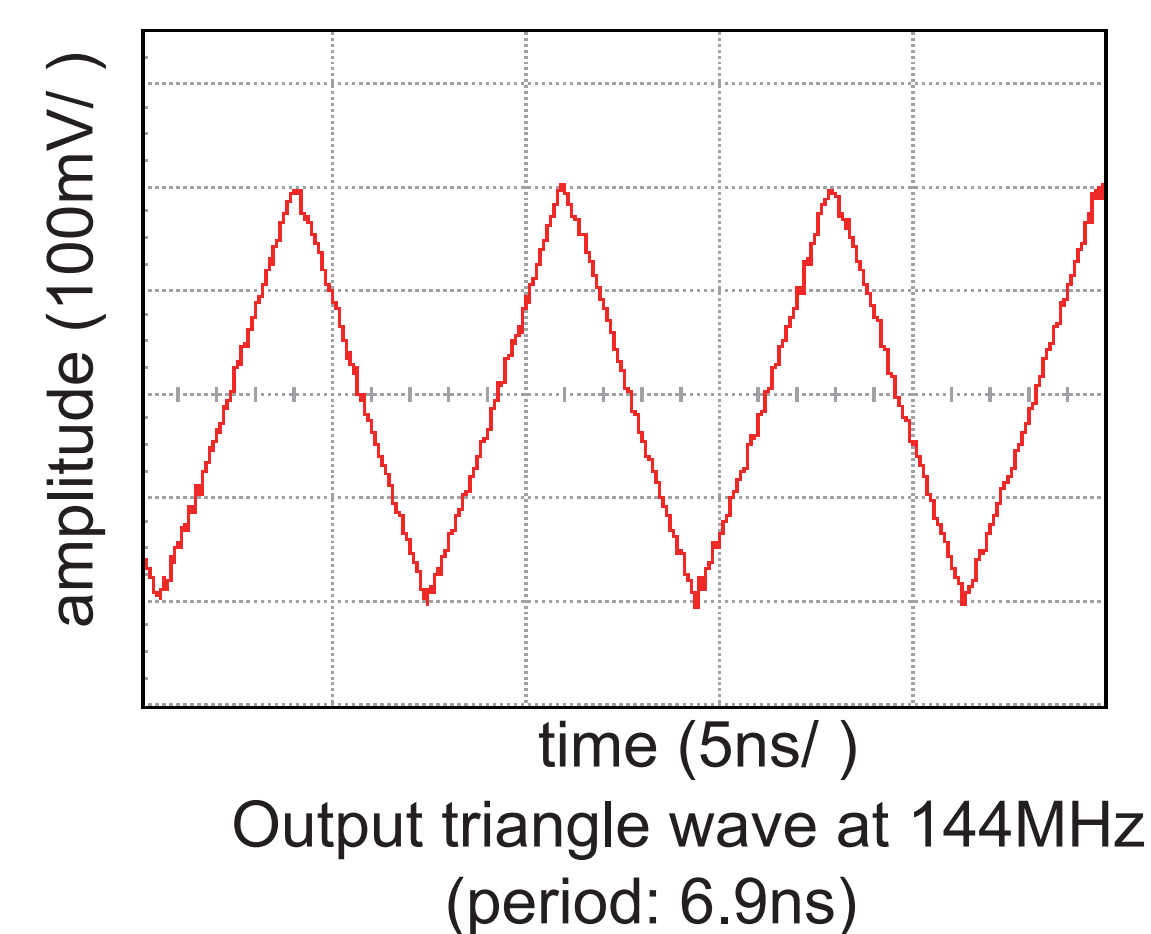
Schematic of the RF Signal Generator

- ◆ Fabricated by 0.18- μm CMOS process
- ◆ Delay element : Two CMOS inverters
The delay is about 70ps.
- ◆ Delay elements : 32(5-bit)
Sinusoidal RF signal : 26 delayed signals are selected and summed.

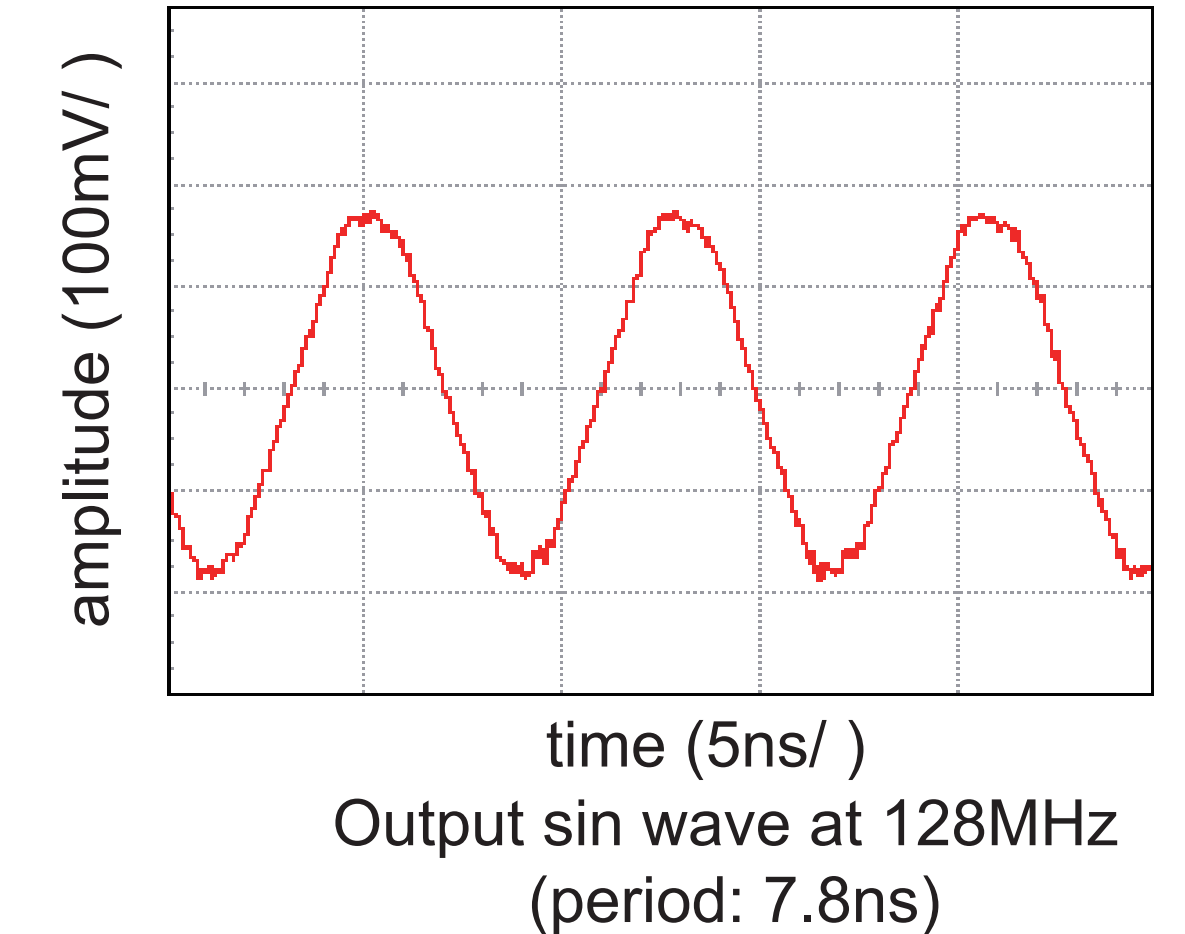


Chip micrograph of the RF Signal Generator (\square : 1mm²)

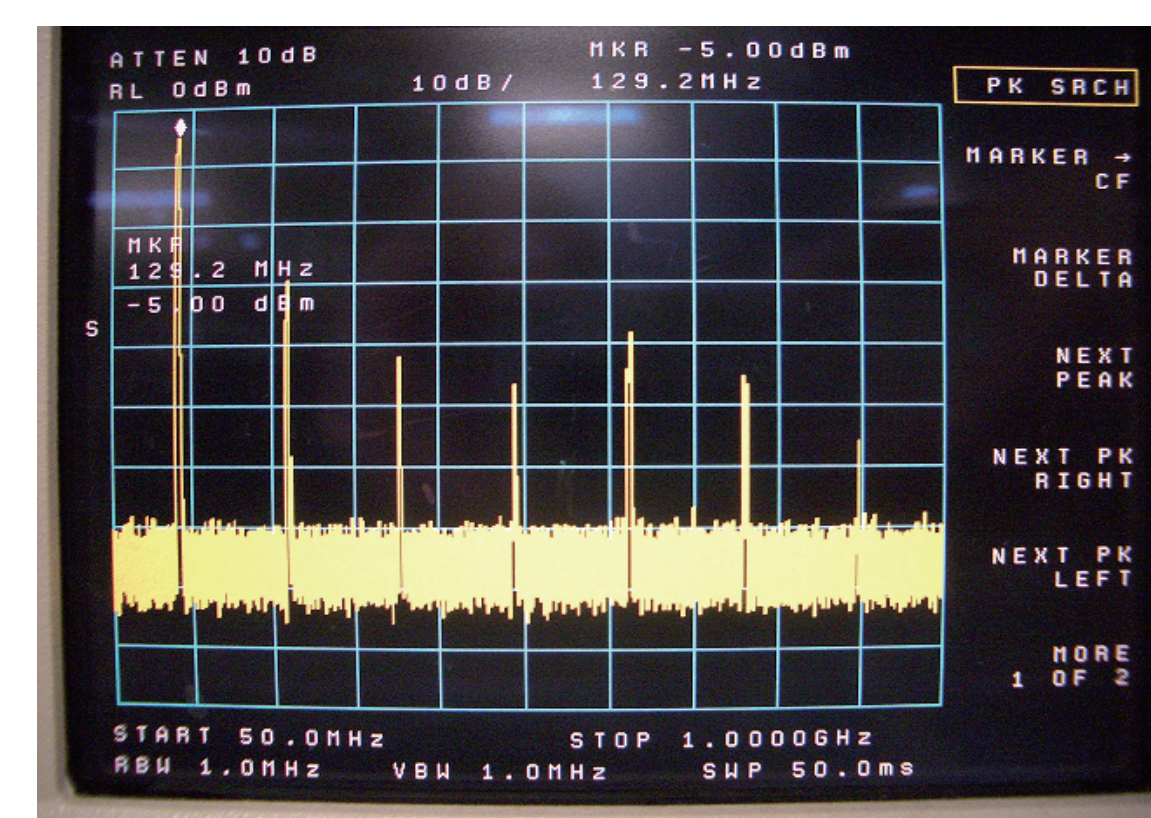
Measurements



Output triangle wave at 144MHz (period: 6.9ns)



Output sin wave at 128MHz (period: 7.8ns)



Measured output spectrum of the harmonics

Performance summary

	Sin wave
Frequency [MHz]	128
Output power [dBm]	-6.6
2 nd harmonics [dBc]	-23
3 rd harmonics [dBc]	-37

4. Conclusion

- The time-to-analog conversion technique for RF signal generation has been suggested.
- RF signal generation was confirmed by fabricating the test chip.

The technique could become particularly attractive in the future .when CMOS become much faster yet the supply is deep-sub-1V.