A Process-Scalable RF Transceiver for Short Range Communication in 90nm Si CMOS

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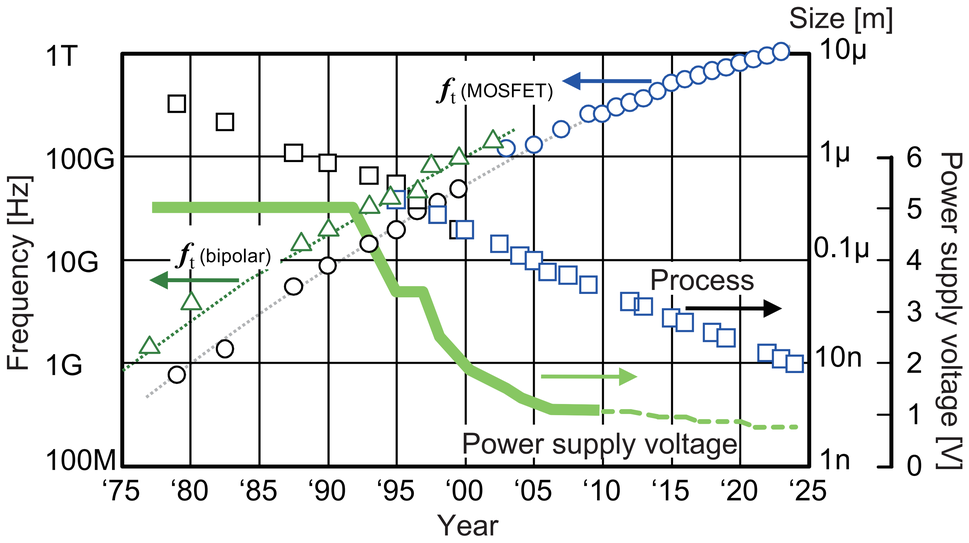
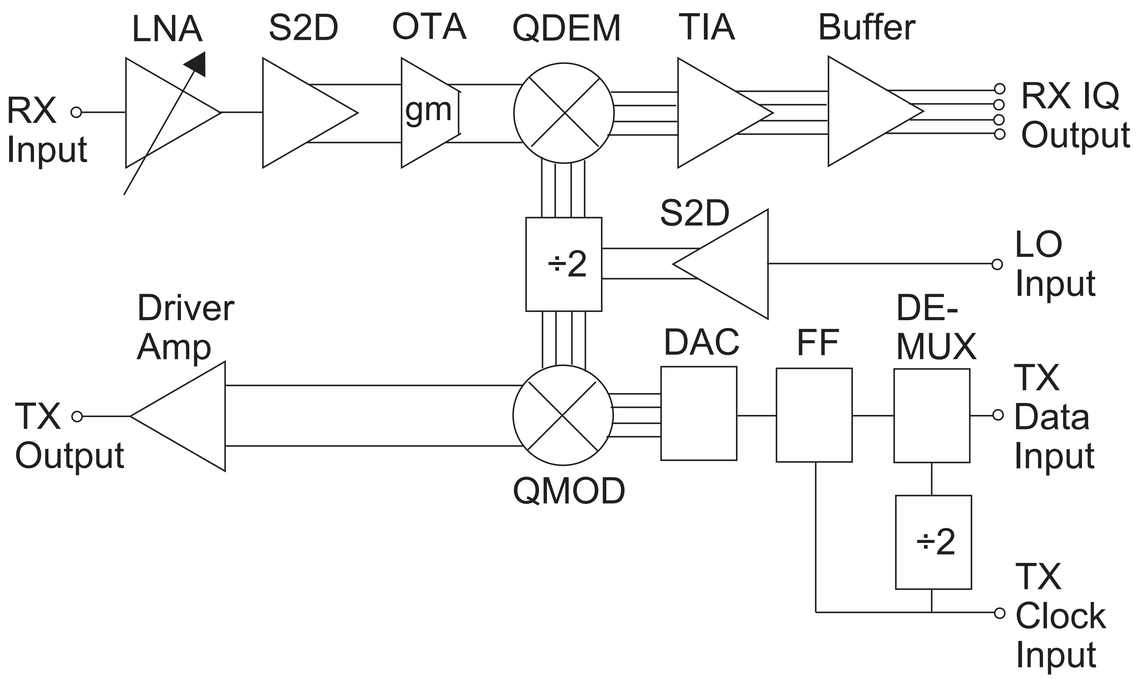
Motivation & purpose



- RF CMOS becomes reality thanks to the process scaling down.
- High speed & high frequency operation can be realized by scaled CMOS.
- However, the area of RF CMOS circuits cannot be shrunk due to huge passive components such as inductors.
- Additionally, supply voltage is below 1V in recent CMOS and must be lowered in finer process.

Purpose is the development of an process-scalable RF transceiver.

Transceiver Architecture

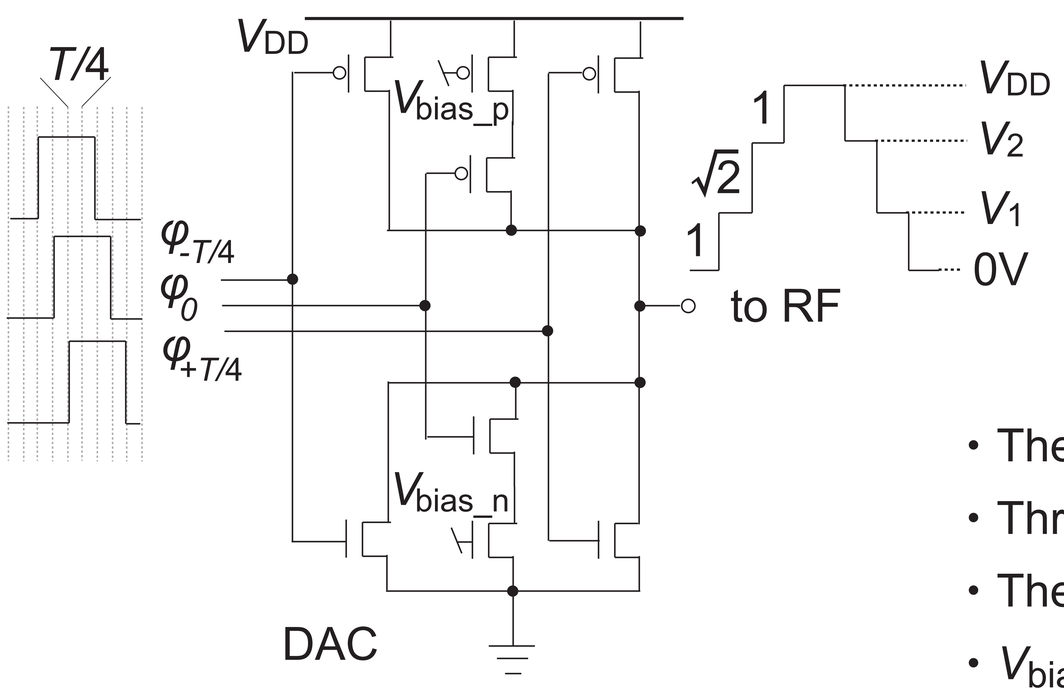


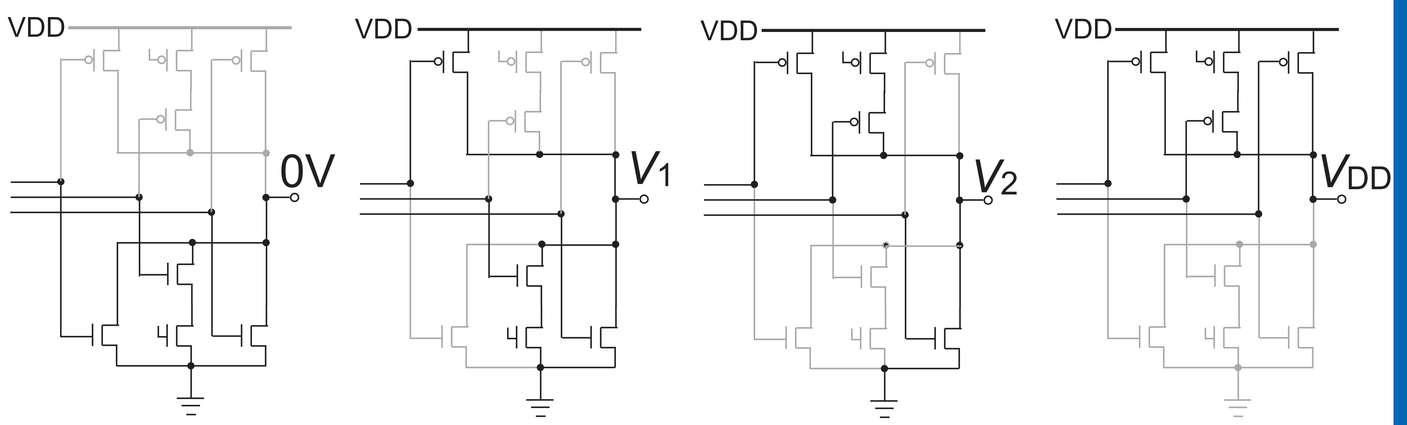
Specifications of test wireless system

Datarate	500Mbps
Modulation	QPSK
Frequency range	0.5~2.5GHz
Distance	Within 1m
Supply voltage	1V

- RX and TX employ direct conversion architecture.
- All circuits are realized without inductor to save the area.
- Inverter-based topology is used for low supply voltage.
- TX baseband part makes 500Mb/s QPSK signal with the sideband suppression.

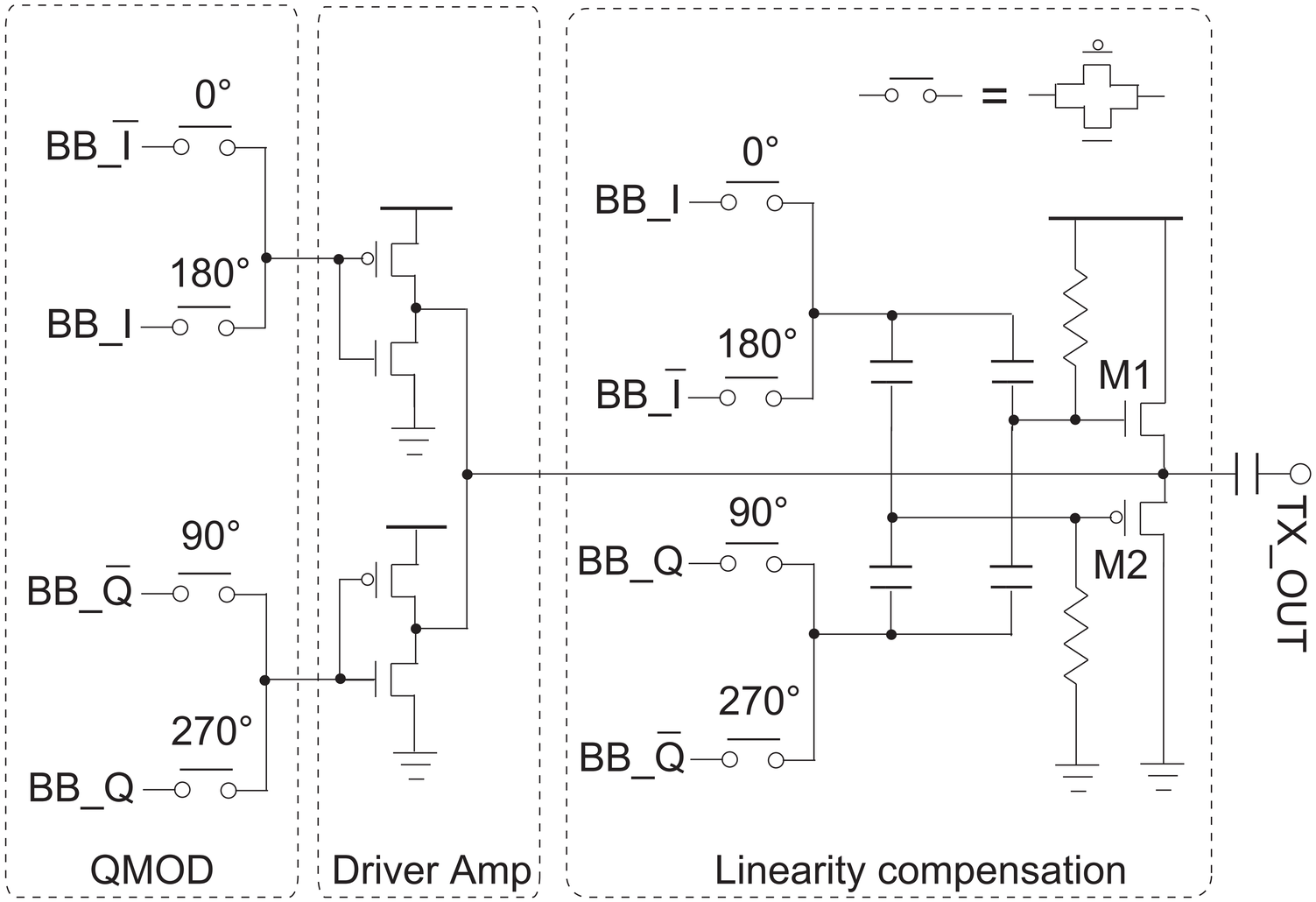
TX baseband



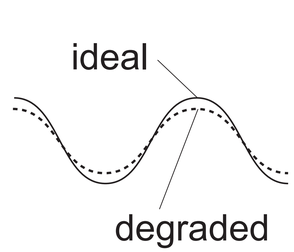


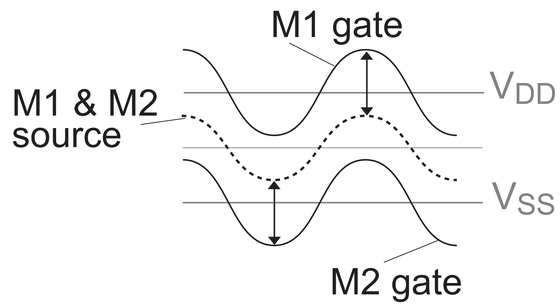
- The baseband part realizes 250Mb/s QPSK symbol signal.
- Three phase shifted symbol signals are input to the DAC.
- The DAC limits the non-desired sideband spectrum by operating above.
- V_{bias_p} and V_{bias_n} is used for the compensation of the process variation.

TX RF

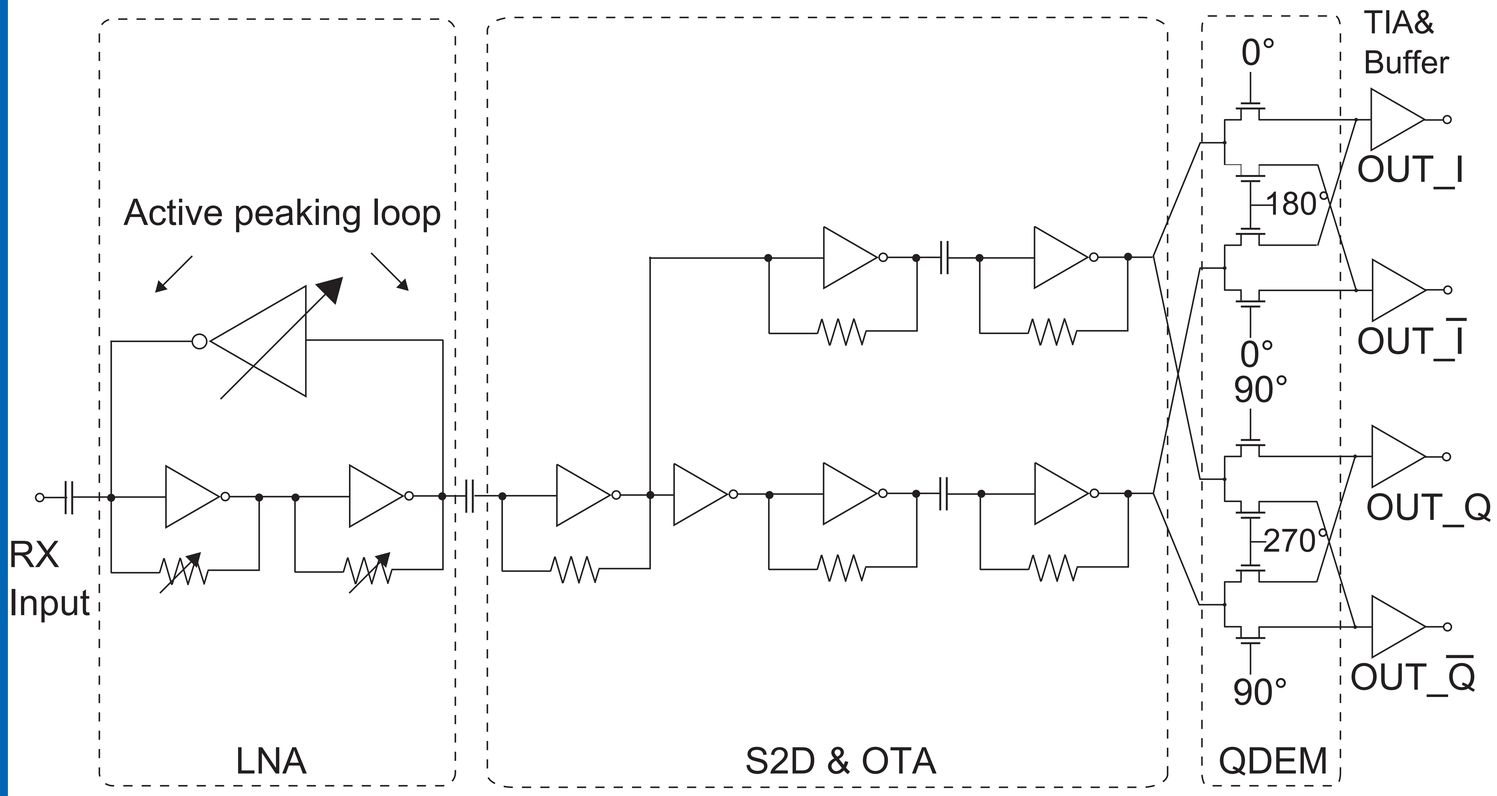


- QMOD is consisting of the complementary switches to realize high linearity and SNR.
- The driver amplifier is inverter-based topology to enlarge the dynamic range without inductor.
- The linearity is compensated around the peak of the driver amplifier output signal.
- The linearity compensation improves the IM3 by 6dB.

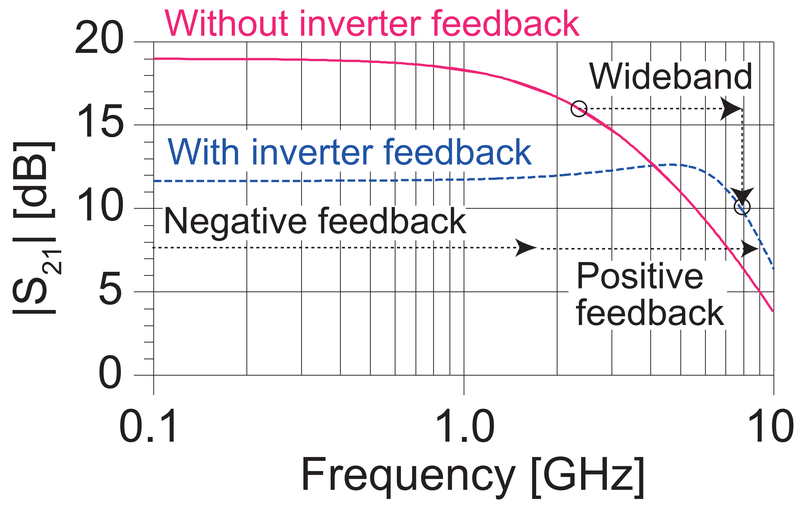




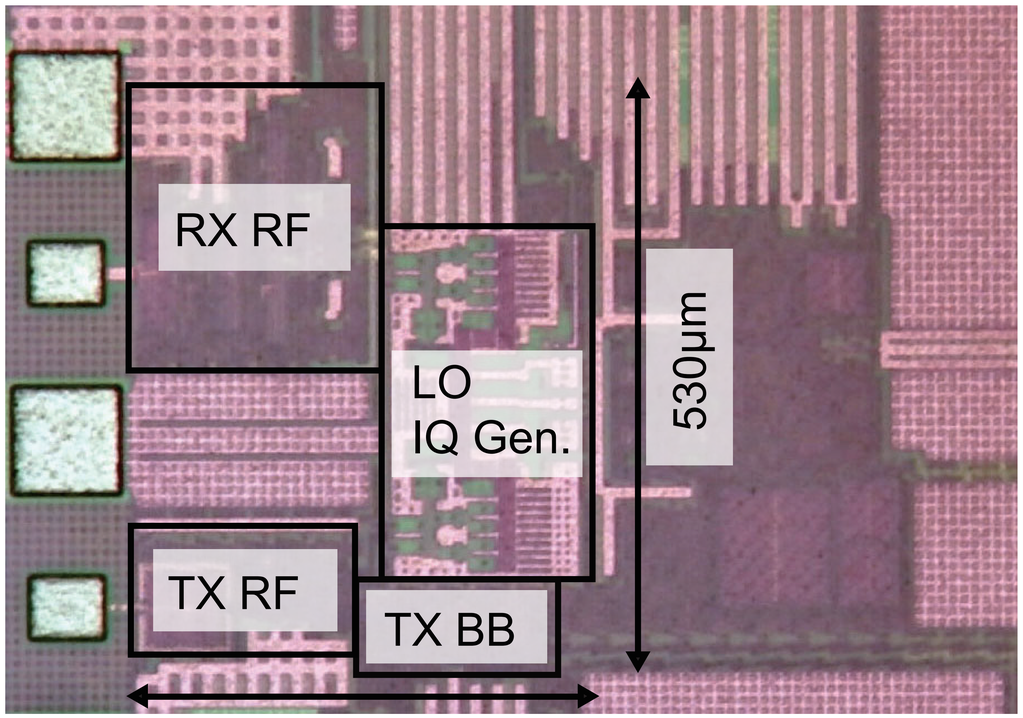
RX



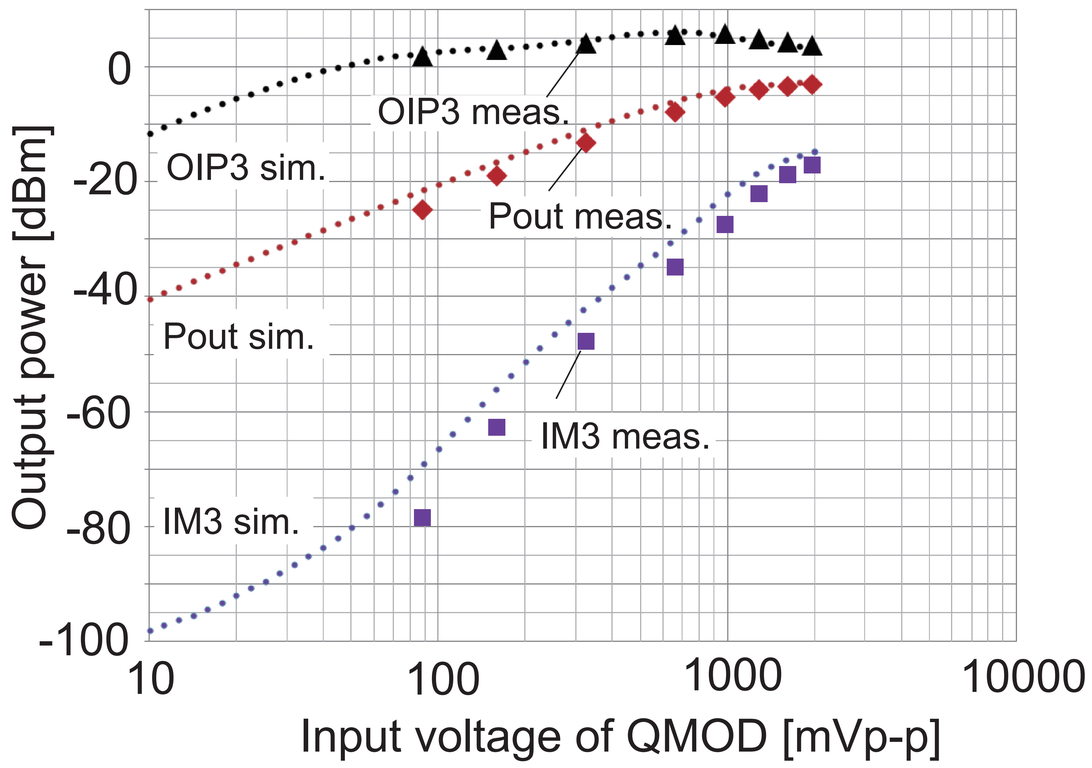
- The receiver is consisting of inverter-based circuits to obtain wide dynamic range with low supply voltage.
- LNA employs cherry-hooper and active peaking technique to broaden the bandwidth and adjust the input impedance.
- LNA has two gain (16&0dB) mode for wide dynamic range.



Measurement results

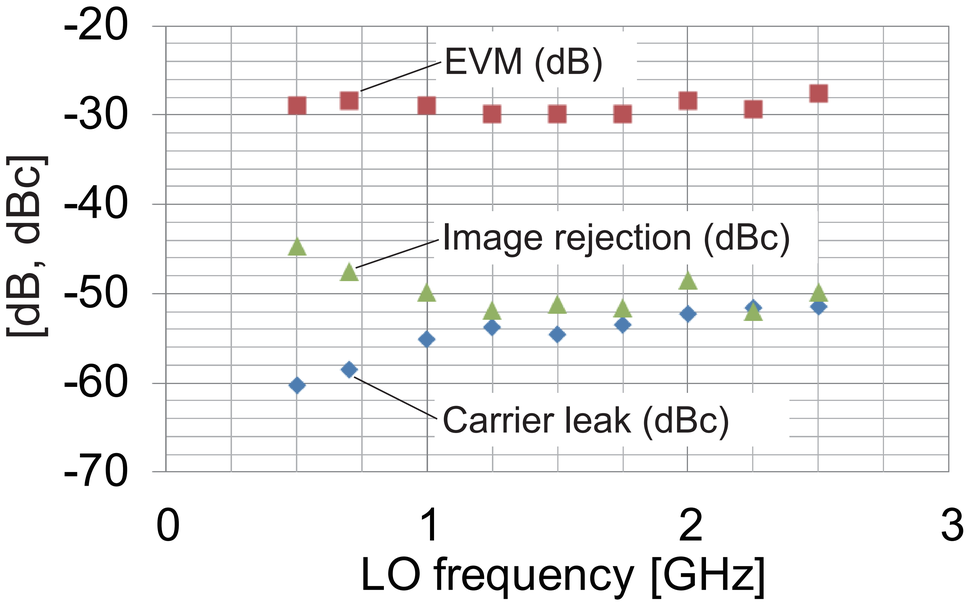


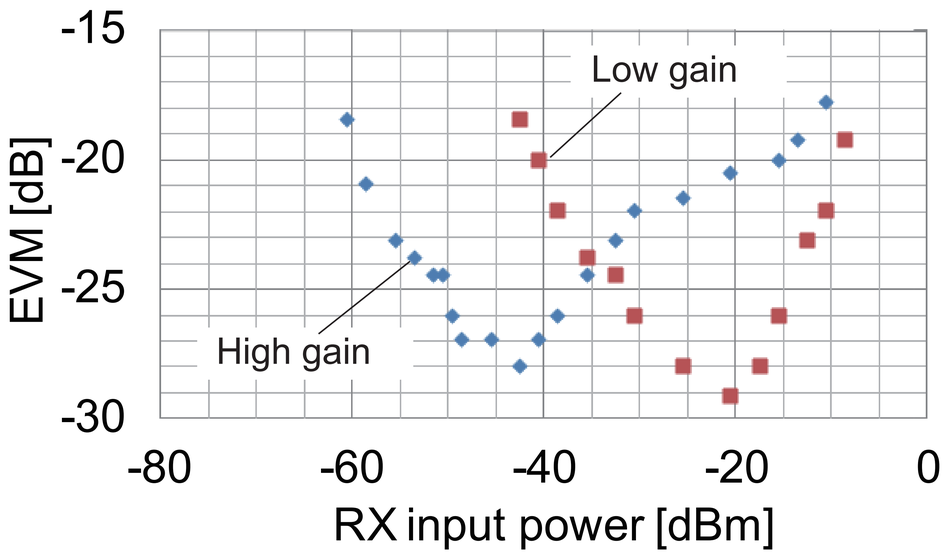
The proposed transceiver was fabricated with 90nm Si CMOS.

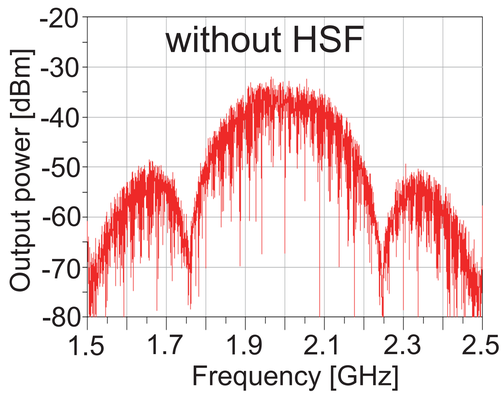


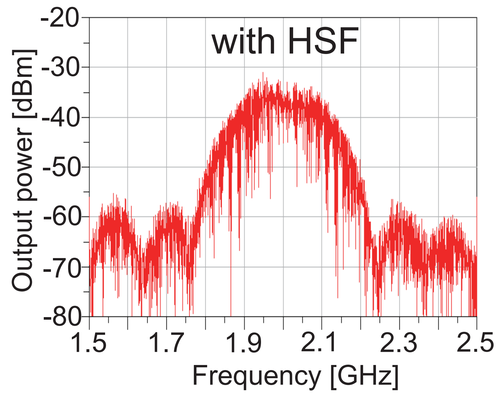
TX sim. & meas. results of OIP3 at 1GHz carrier

Measurement results



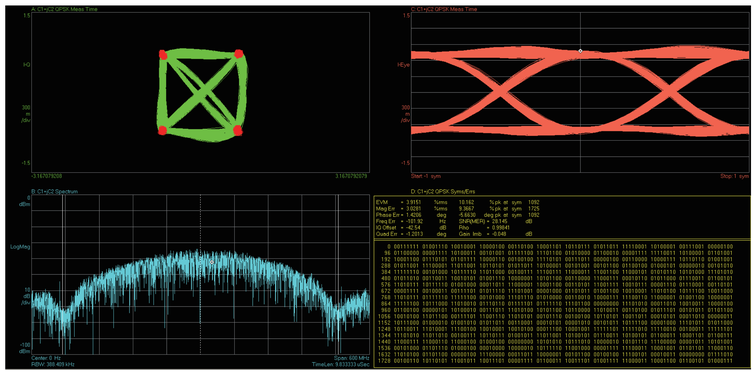






QPSK modulated spectrum at 500Mb/s with or without the adjustment of the bias in DAC.

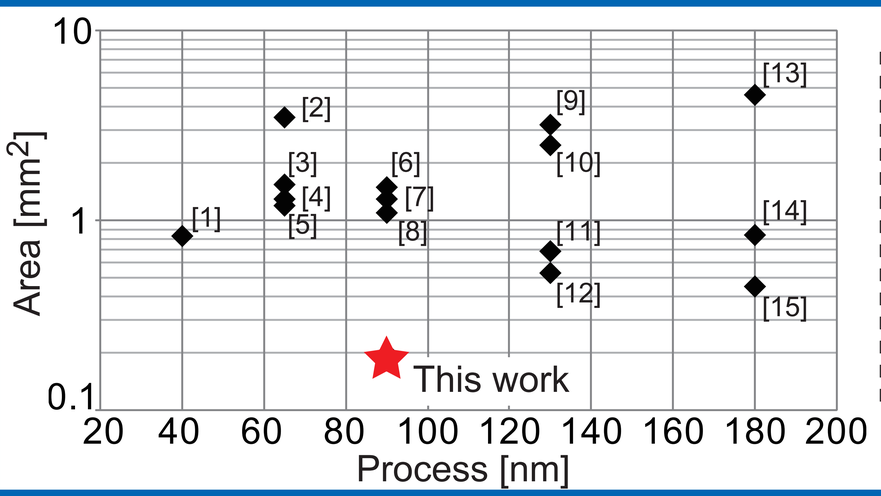
HSF:High speed filtering



Measurement results of the demodulated signals at high gain mode, -43dBm input power, 1GHz carrier, 500Mb/s datarate and PRBS11.

Supply voltage	1V
Datarate	500Mb/s
Power consumption	TX:11.9mW, RX:35.3mW, Lo and RX Buffer: 35mW
Frequency range	TX:0.5~2.5GHz, RX:0.5~1.5GHz
RX sensitivity	-60dBm at EVM= -20dB
RX dynamic range	50dB
TX output power	-5dBm with EVM= -28dB
Active area	0.2mm^2

Conclusion



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- We proposed a process-scalable RF transceiver with inductor-less and inverter-based circuits.
- The transceiver employs the linearity compensated technique in TX and cherry-hooper and active peaking technique in RX.
- The prototype transceiver was fabricated in 90nm Si CMOS.
- The transceiver realized 500Mb/s communication with 1V supply voltage and the area of 0.2mm^2.