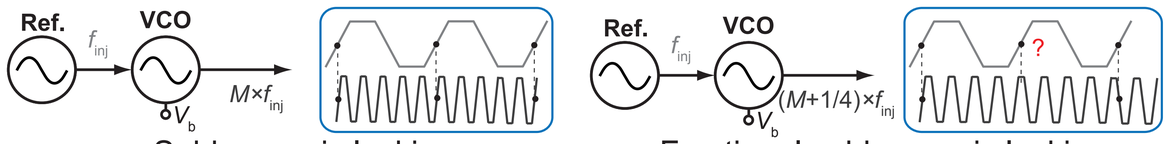
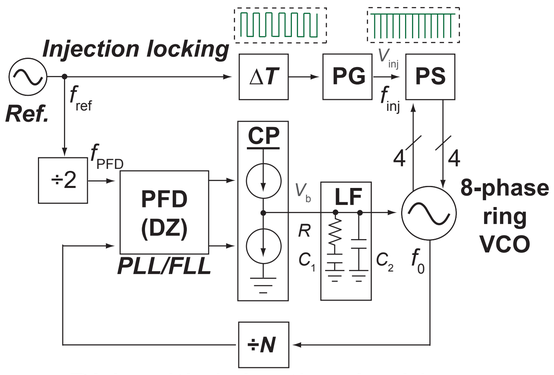
Fractionally Injection-Locked Frequency Synthesizer

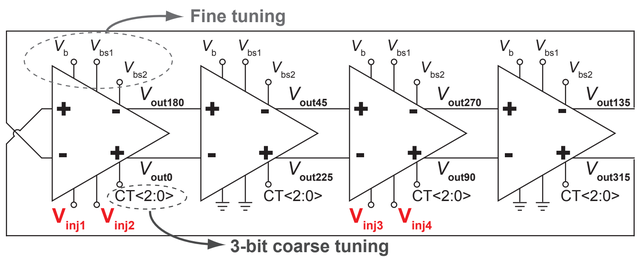
Motivation:Low phase-noise without LC



Proposed Frequency Synthesizer

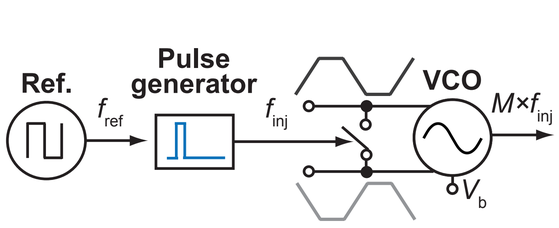


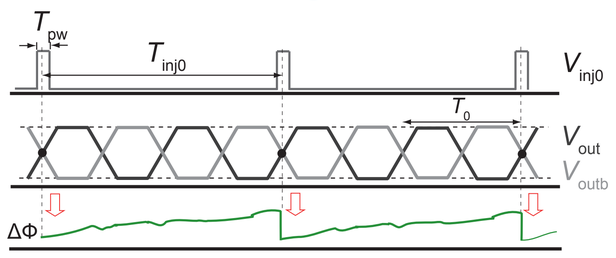
PLL with injection locking



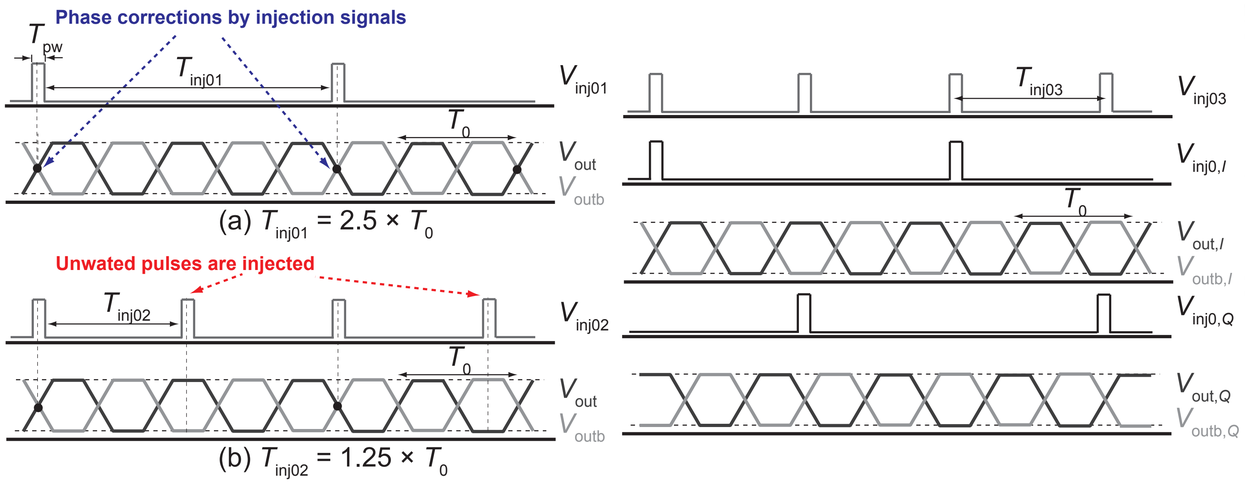
8-phase ring VCO

Conventional Subharmonic Locking

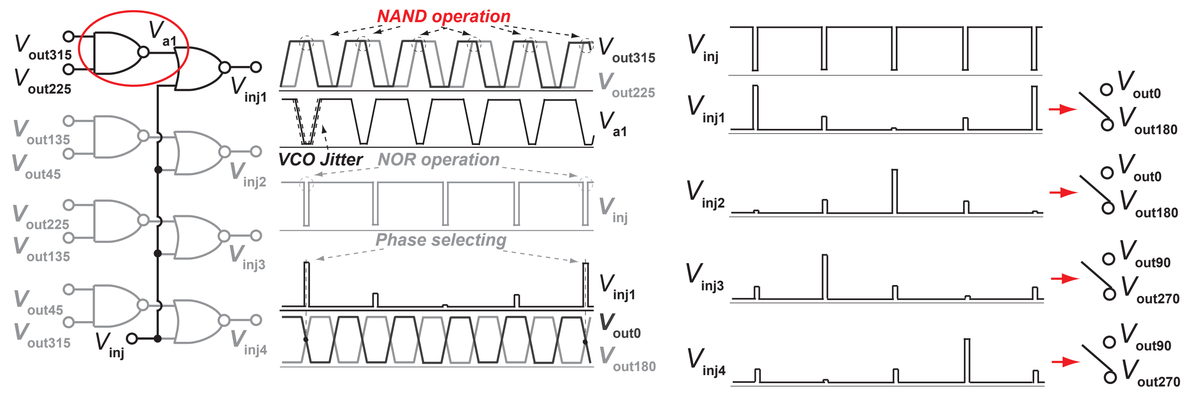




Fractional Subharmonic Locking

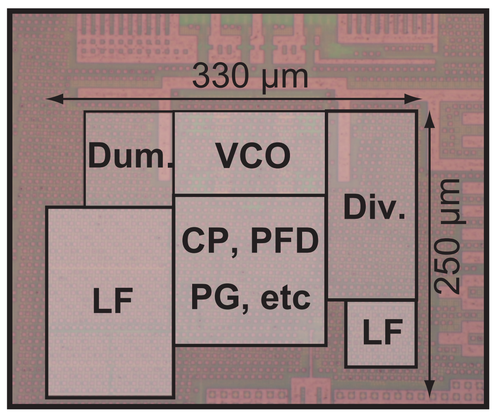


Proposed Pulse-Selection Technique

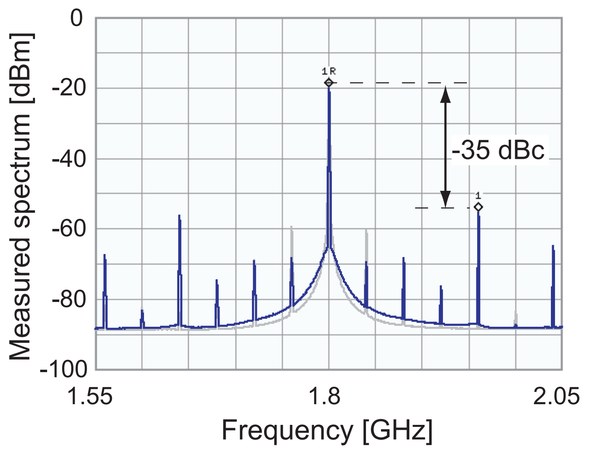


Pulse for injection locking

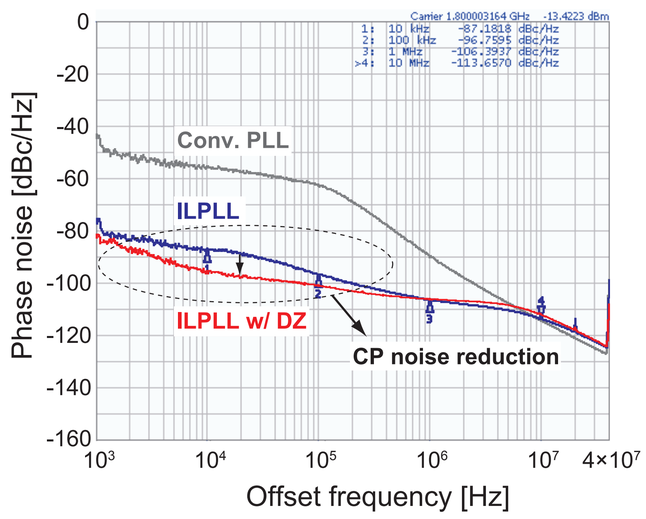
Measurement Results



Process	90 nm CMOS	
Supply voltage	1.0 V	
Input frequency (f_{ref})	80 MHz	
Injection frequency (f_{inj})	160 MHz	
Output frequency (f_0)	1.8 GHz	2.0 GHz
f_0/f_{inj}	11.25	12.5
Phase noise@ 1 MHz	-106 dBc/Hz	-103 dBc/Hz
Power consumption	22 mW (w/ I/O buffers)	
	VCO: 50% Injection path: 36% PLL blocks: 14% {19 mW (sim.), w/o I/O buffers}	



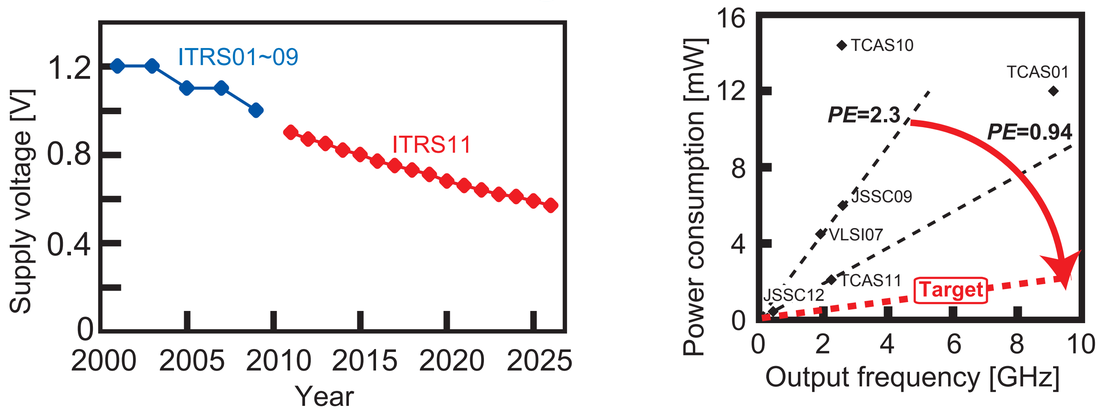
Output signal spectram



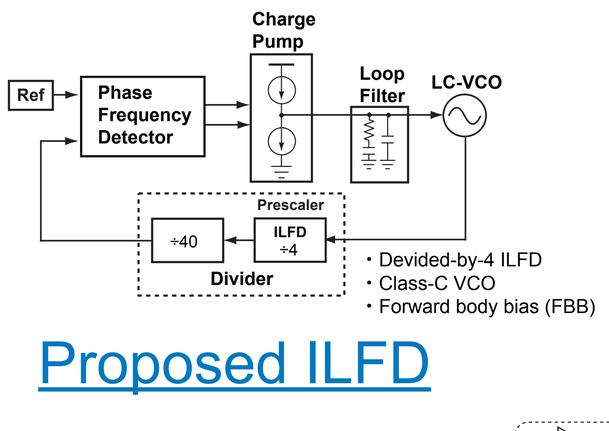
Phase noise

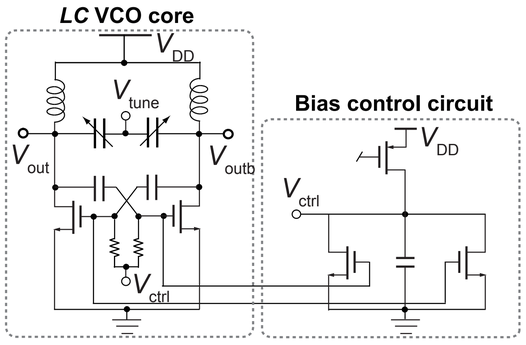
Ultra-Low-Power Frequency Synthesizer

Motivation:Low voltage operation

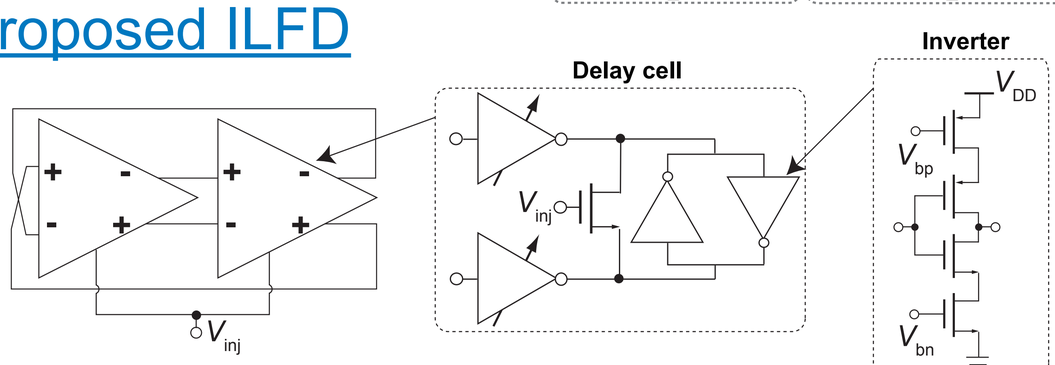


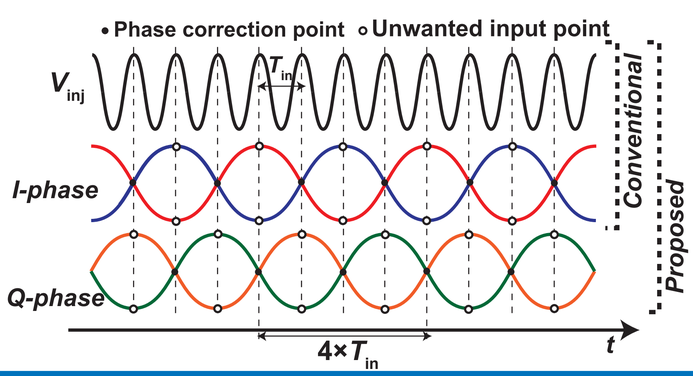
Proposed Frequency Synthesizer

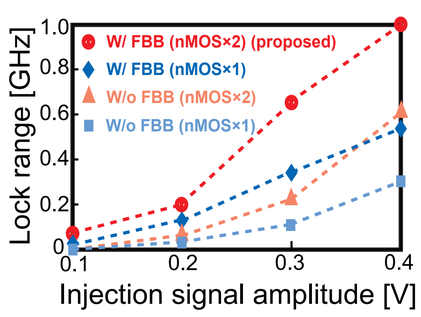




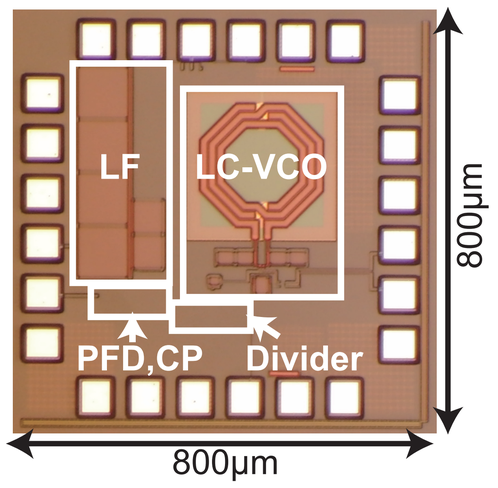
Proposed ILFD

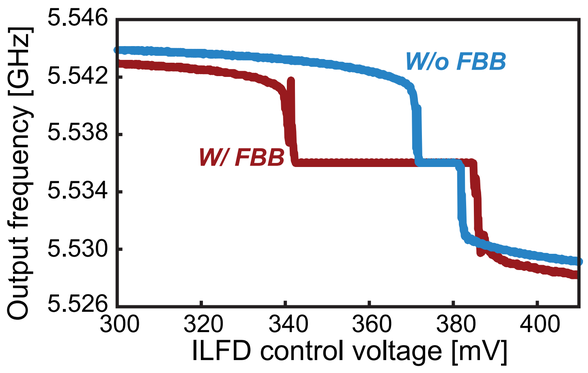


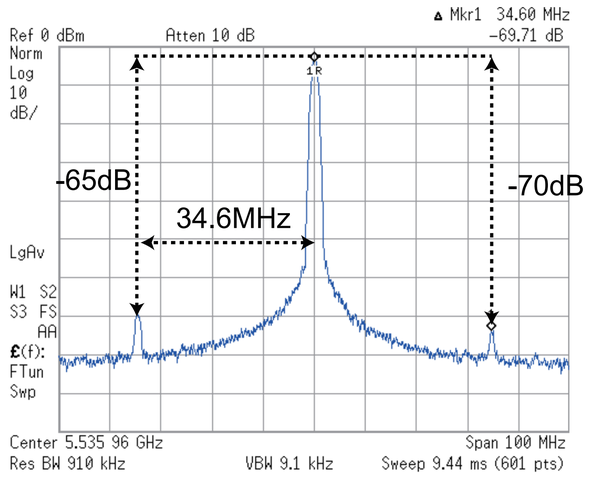




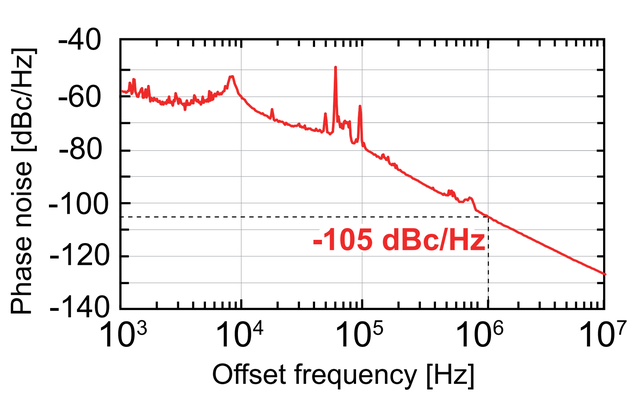
Measurement Results







Output signal spectram



	Tech. [nm]	f_{out} [GHz]	V_{DD} [V]	PN [dBc/Hz]	Power [mW]
This work	65	5.54	0.5	-105	1.6
[1]	180	1.9	0.5	-120	4.5
[2]	180	2.56	0.5	-105	14.4
[3]	90	2.59	0.5/0.65	-113	6.0
[4]	130	9.12	0.5/0.8	-105	12
[5]	90	2.24	0.5	-87	2.1

[1] H.-H. Hsieh, et al., VLSI 2007
[2] C.-T. Lu, et al., TCAS 2010
[3] S.-A. Yu, et al., JSSC 2009
[4] C. -Y. Yang, et al., TCAS 2001
[5] K. -H. Cheng, et al., TCAS 2011