High Performance Scalable RF-CMOS Integrated Circuit Design

Green ICE Tokyo Tech — Information Communication Energy
Semiconductor Solution Research

Tokyo Institute of Technology,
Solutions Research Lab., Masu Lab.
http://masu-www.pi.titech.ac.jp/

Motivation:Scalable/Inductorless

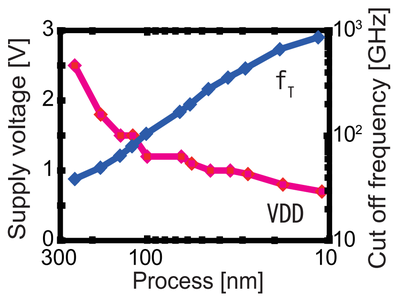
CMOS Process Scaling

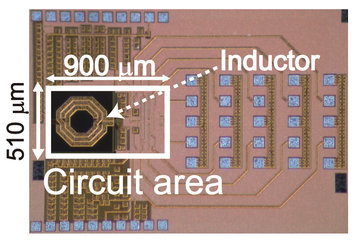
[advantages]

RF circuit become CMOS,digital assisted,SoC

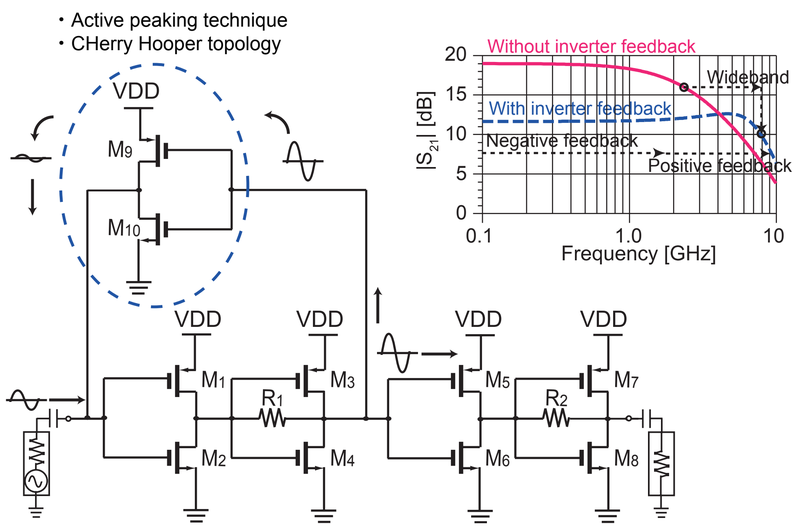
[problems]

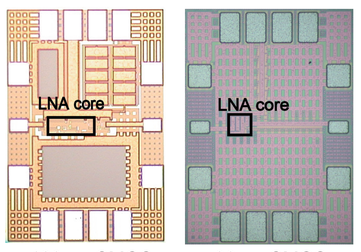
falling supply voltage　　difficult to small area





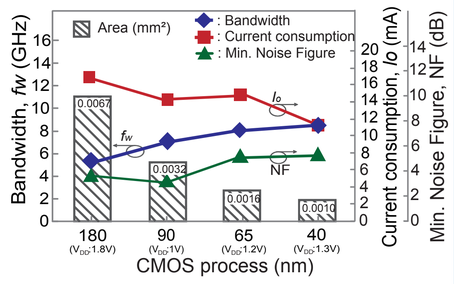
Scalable Wideband Inverter-Based LNA

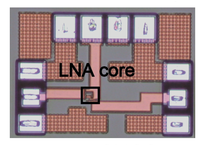




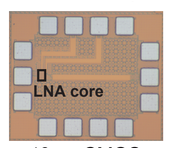
180nm CMOS
Vdd: 1.8 V
Size: 45 ×148μm^2

90nm CMOS
Vdd: 1.0 V
Size: 54 ×60μm^2





65nm CMOS
Vdd: 1.2 V
Size: 40 ×40μm^2



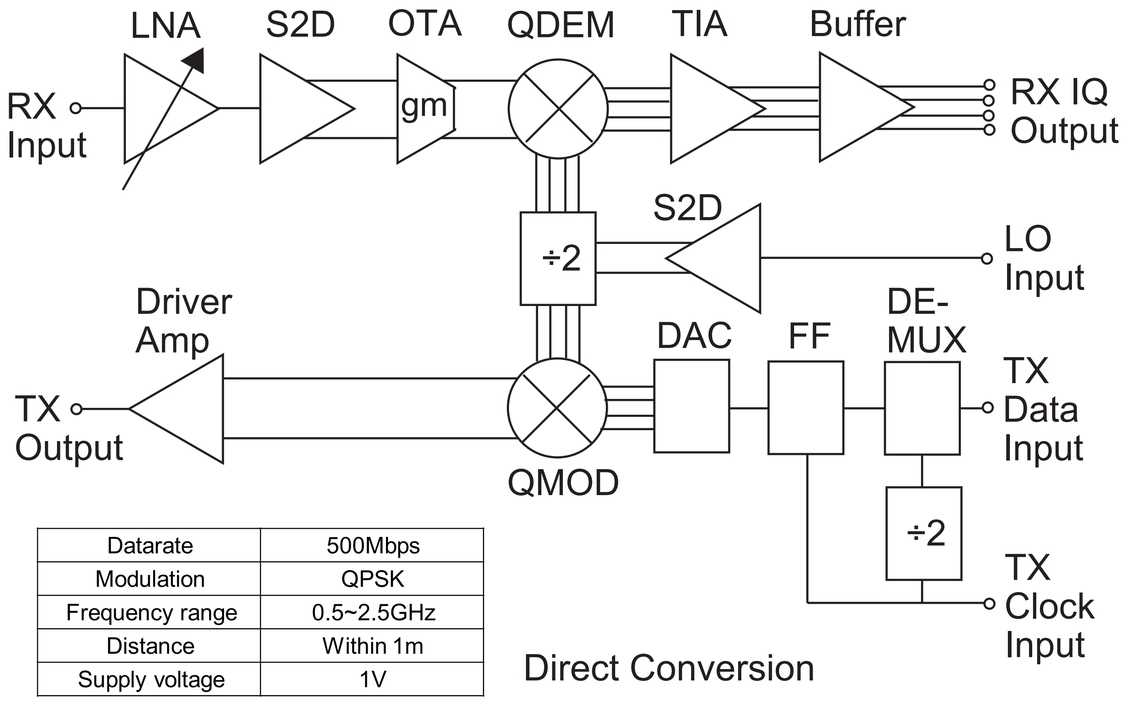
40nm CMOS
Vdd: 1.3 V
Size: 25 ×40μm^2

40nm CMOS

Bandwidth	1.0 – 8.0 GHz
Gain	17.5 dB
Min. NF	5.1dB
IIP3	-9.2 dBm
Power	14.3 mW

A Process-Scalable RF Transceiver

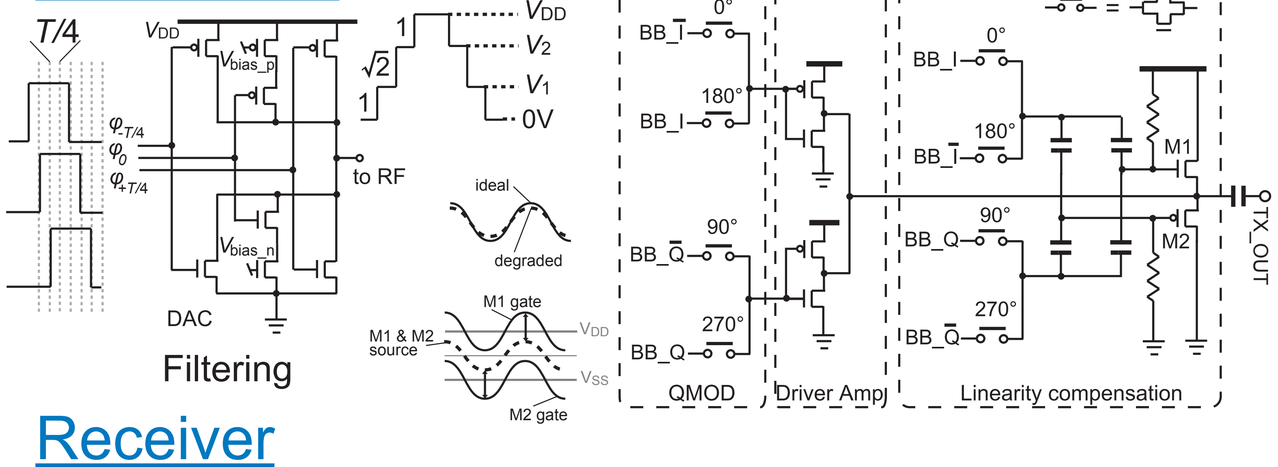
Transceiver Architecture



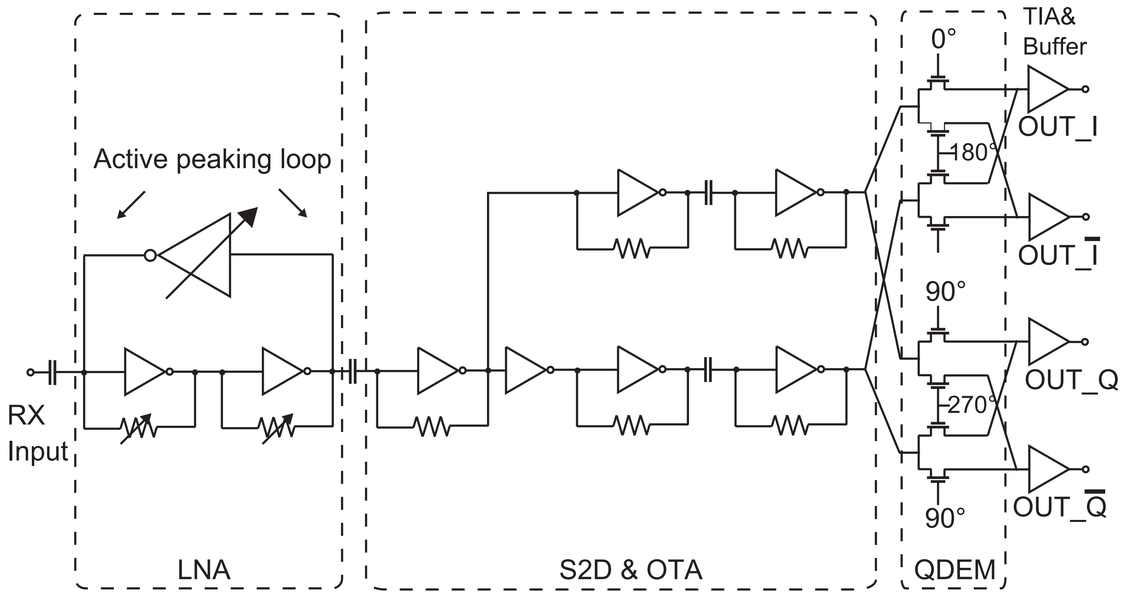
Datarate	500Mbps
Modulation	QPSK
Frequency range	0.5~2.5GHz
Distance	Within 1m
Supply voltage	1V

Direct Conversion

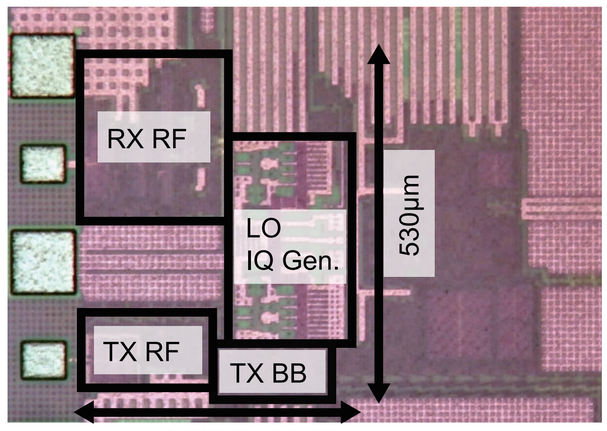
Transmitter



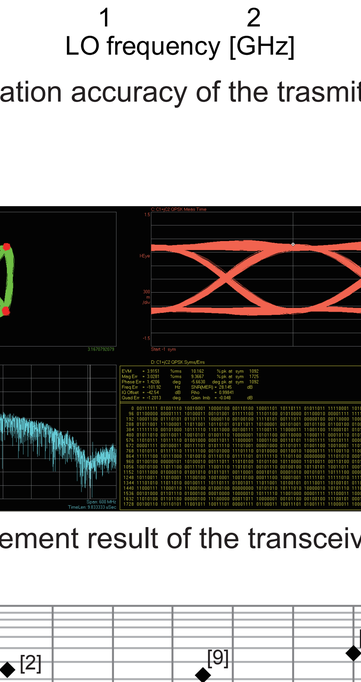
Receiver



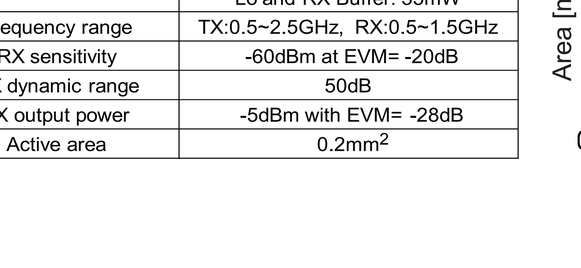
Measurement Results



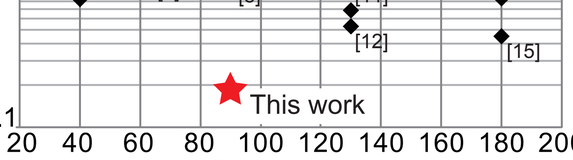
Fablicated with 90nm Si CMOS



HSF:High speed filtering



Two-tone test at 1GHz carrier



Modulation accuracy of the trasmitter

EVM versus RX input power

Measurement result of the transceiver

Supply voltage	1V
Datarate	500Mb/s
Power consumption	TX:11.9mW, RX:35.3mW, Lo and RX Buffer: 35mW
Frequency range	TX:0.5~2.5GHz, RX:0.5~1.5GHz
RX sensitivity	-60dBm at EVM= -20dB
RX dynamic range	50dB
TX output power	-5dBm with EVM= -28dB
Active area	0.2mm^2