Optimal Design Method for Chip-Area-Efficient CMOS Low-Dropout Regulator

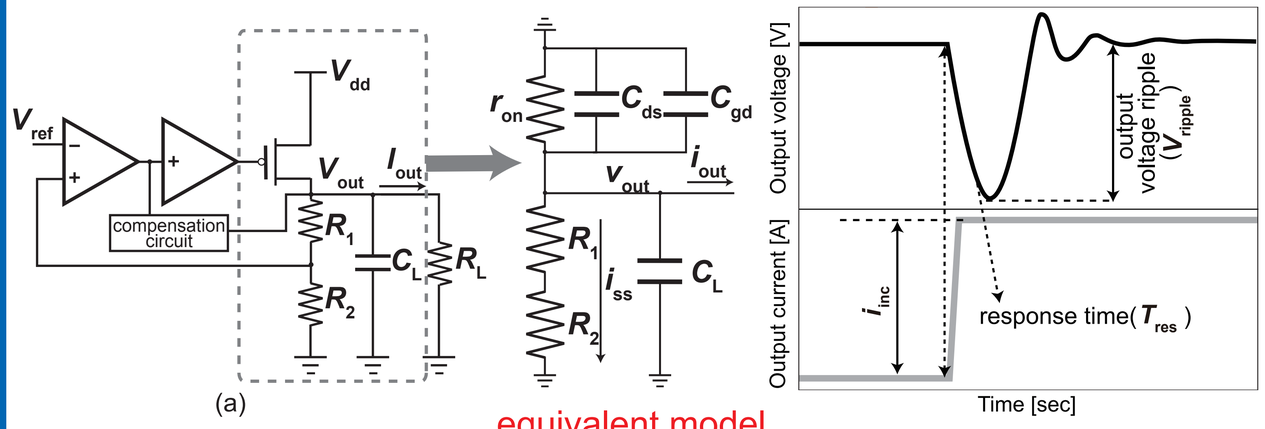
Sho Ikeda, Hiroyuki Ito, Noboru Ishihara, and Kazuya Masu
Solutions Research Laboratory, Tokyo Institute of Technology

Background

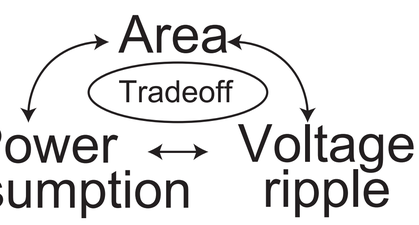
- RF wireless communication circuit
  - unstable voltage of battery
  - performance degration of supply voltage perturbation
  - LDO(Low DropOut regulator) is needed
- RF module SoC
  - full-integration without external component
  - Large capacitor is needed for LDO

<u>LDO with small chip area is required</u>

Purpose

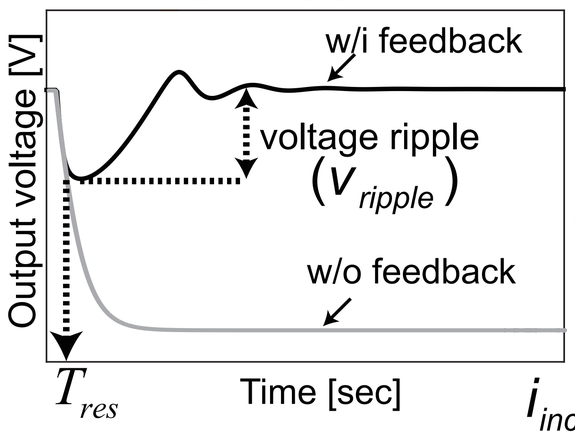


<u>Optimal design method for small area</u>



Detail analysis

- voltage ripple



$$v_{out} = -\frac{i_{out}}{h + s(C_L + C_{gd} + C_{ds})}$$

$$\left(i_{out}(s) = \frac{i_{inc}}{s}, h = \frac{1}{R_1 + R_2} + \frac{1}{r_{on}} \right)$$

i_{inc} :increment of output current

when r_{on} is constant

$$v_{ripple} = \frac{i_{inc}}{h}\left[\exp\left(-\frac{h}{C_L + C_{gd} + C_{ds}} T_{res}\right) - 1\right]$$

v_{ripple} can be determined by T_{res}

- Response time

$$A_{open}(s) = \frac{A_0}{\left(1 + s/\omega_1\right)\left(1 + s/\omega_n\right)}$$

2nd order approximation

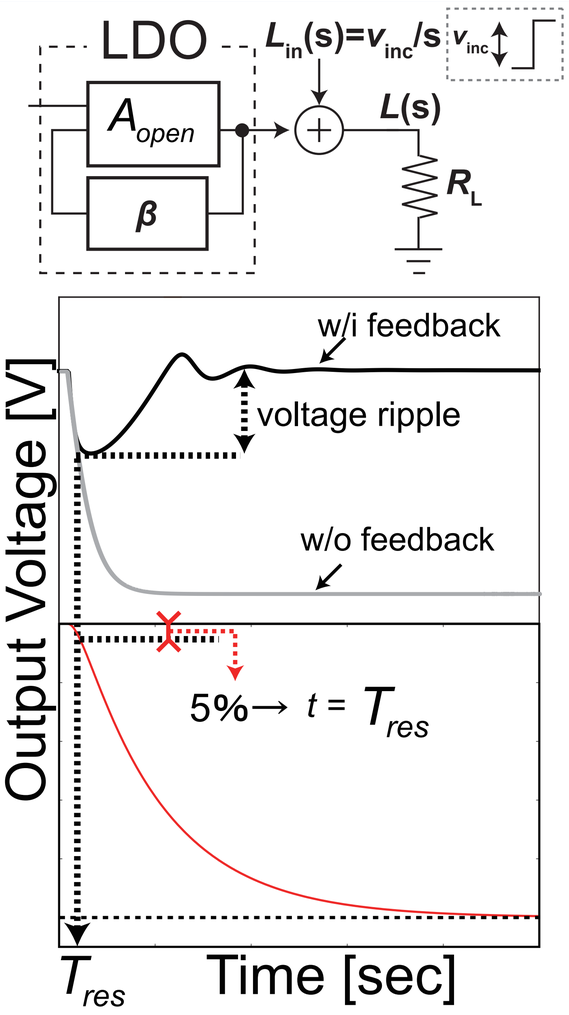
ω_1 :dominant-pole ω_n :nondominant-complex-pole

$$L(s) = \frac{1}{1 + \beta A_{open}(s)} L_{in}(s)$$

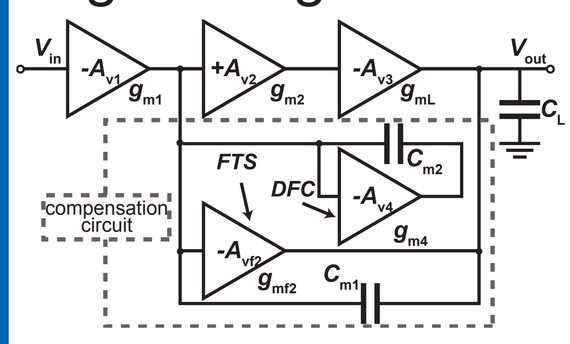
β : feedback resistance

$$T_{res} = \frac{\pi}{5\sqrt{\left|4\beta A_0 \omega_1 \omega_n - \omega_1^2\right|}}$$

approximate the response time by the voltage step response



- gain stage

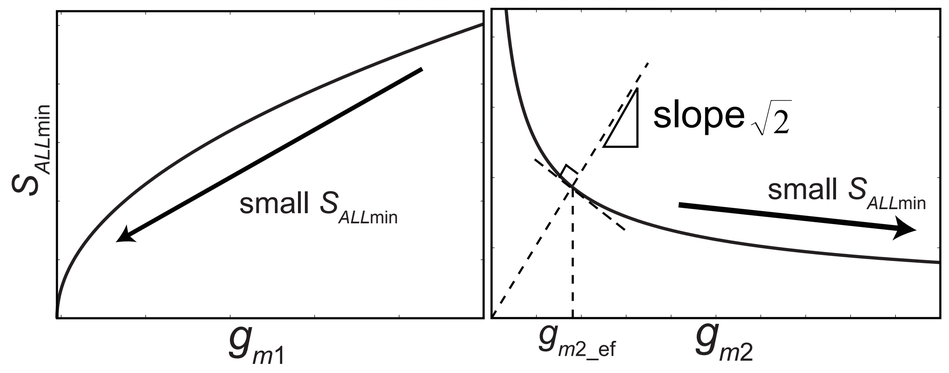


$$S_{ALL} = W_{pass}L_{pass} + \frac{1}{C_{MIM}}(C_{m1} + C_{m2}) + \frac{C_L}{C_{MOS}}$$

$$= \frac{a}{g_{m2}C_L} + \left(bg_{m1} + \frac{1}{C_{MOS}}\right)C_L$$

$$\geq 2\sqrt{\frac{a}{g_{m2}}\left(bg_{m1} + \frac{1}{C_{MOS}}\right)}$$

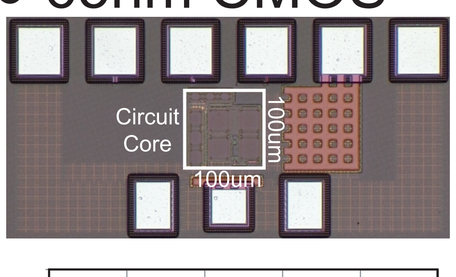
the minimum value of area



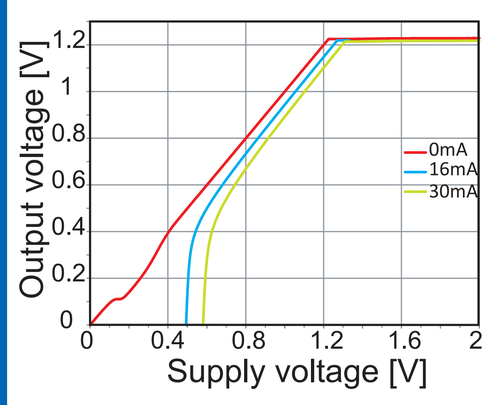
the optimal value of g_{m1} and g_{m2} can be obtained

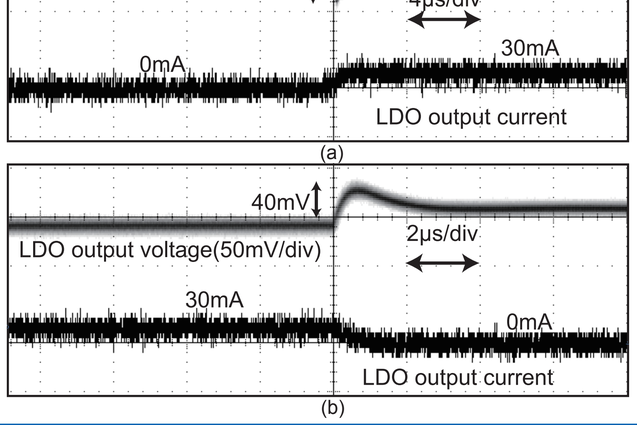
Experimental result

- 65nm CMOS



Supply voltage	1.3V - 1.8V
Output voltage	1.2V
Output current	0mA - 30mA
Core Area	100μm*100μm
Quiescent consumption	472μW





Conclusion

- Optimal LDO design method to minimizing the chip area was proposed.
- To verify the proposed method, LDO was designed and fabricated in 65nm CMOS.