Efficient Power Combining Techniques for CMOS Power Amplifiers

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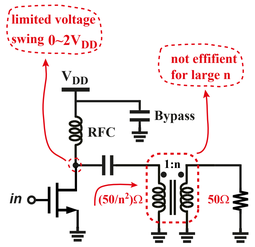
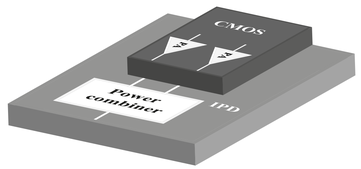
Background

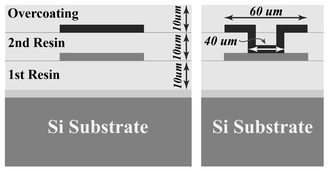
- Why CMOS PA?
  - The lowest cost, the highest integration
  - Fully integrated CMOS PA is a bottleneck.
- Challenges
  - Low breakdown voltage
  - Lossy passives
  - Watt-level CMOS PAs call for advanced techniques



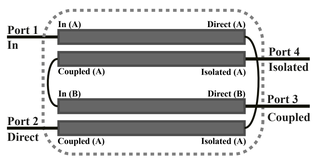
IPD-based power combining: 60 GHz

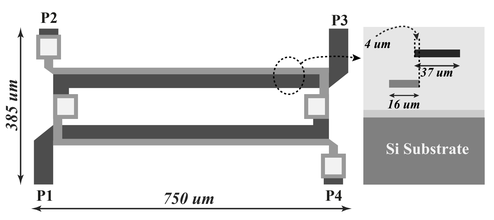
- IPD (Integrated Passive Device) technology
  - Hybrid use of a CMOS chip and an IPD chip
  - Solid ground plane; Thick and wide lines
  - Conventional couplers: big, poor performance

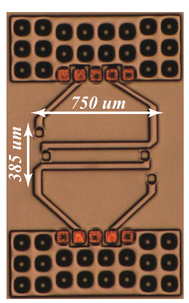




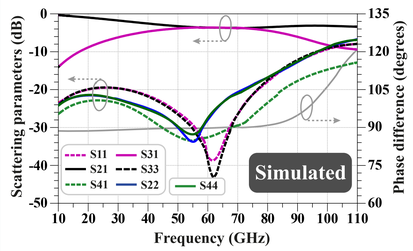
- Tandem coupler
  - Each coupler: -8.34 dB
  - Edge-coupled lines: looser broadside ones: tighter

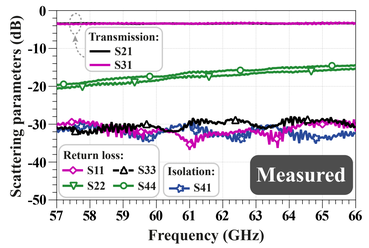






Tandem coupler: results





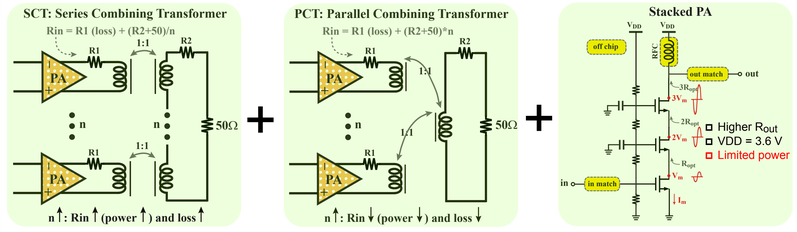
Ref.	BW (GHz)	Tech.	RL (dB)	IL (dB)	Iso. (dB)	Phase error (deg.)	Amp. Imb. (dB)	Area (mm^2)
This work	**57-66**	**Silicon IPD**	**27.9**	**0.67**	**29.7**	**3.7**	**0.31**	**0.288**
[1]	57-66	CMOS	17	4.5	19	8	2	0.083
[2]			18	3	14	5.8	1	0.102
[3]	57-64	Glass IPD	15	2	15	0.5	1.2	0.438
[4]	57-63	MEMS	18	1.1	18	4.37	0.55	1.580

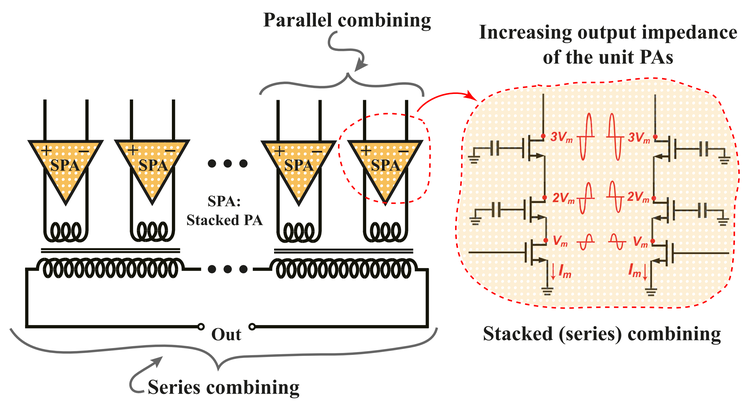
[1] Electronics letters, 2011 [2] IEEE MWCL, 2010 [3] IEEE trans. comp. packag., 2012 [4] MTT-S digest, 2004

- The lowest reported insertion loss and amplitude imbalance
- Area is lower compared to the same technology

A PA with series-parallel transformer

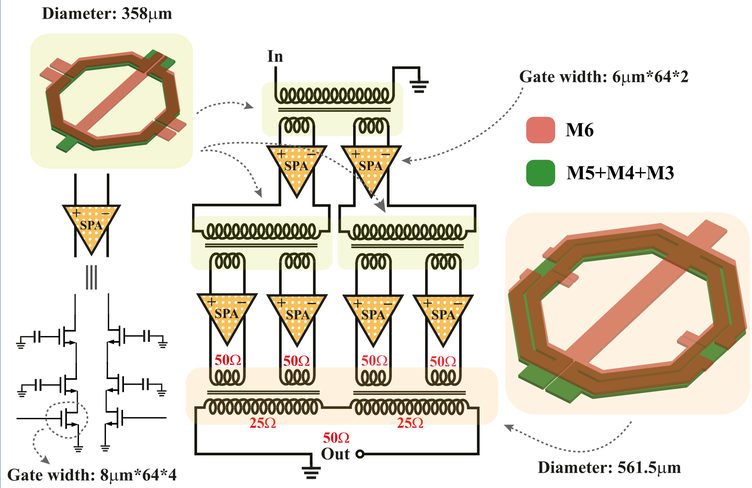
- Concept
  - Exploiting merits of various on-chip power combining methods



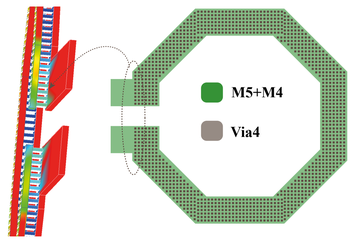


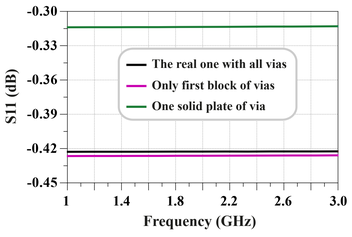
Example: A 2.2 watt CMOS PA

- Eight-way combiner
  - Broadside transformers are used for better coupling.
  - On 180nm CMOS; only thin-oxide transistors are used.
  - Class AB; a splitter netwrok is also designed.



- Effcient and accurate simulation of stacked-metal inductors





- Simulation results