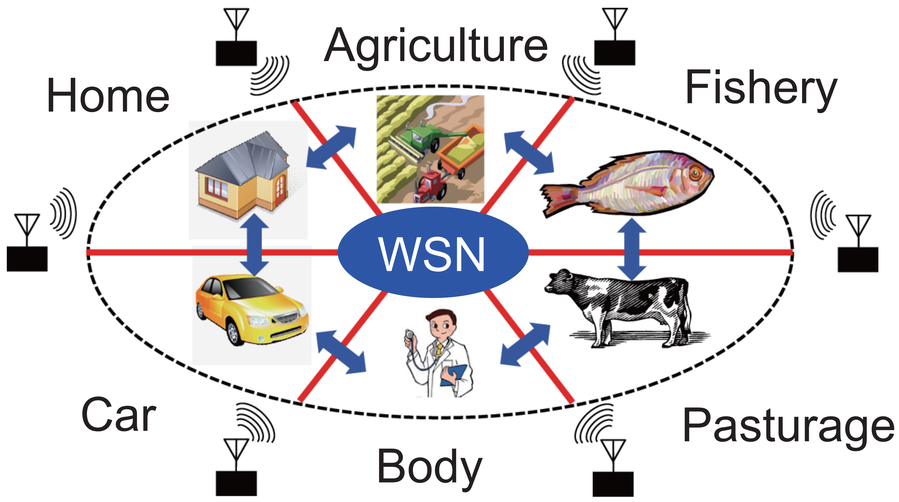
A Sub-1mW 5.5-GHz PLL with Digitally-Calibrated ILFD and Linearized Varactor for Low Supply Voltage Operation

Sho Ikeda, Tatsuya Kamimura, Sangyeop Lee, Hiroyuki Ito, Noboru Ishihara, and Kazuya Masu
Solutions Research Laboratory, Tokyo Institute of Technology

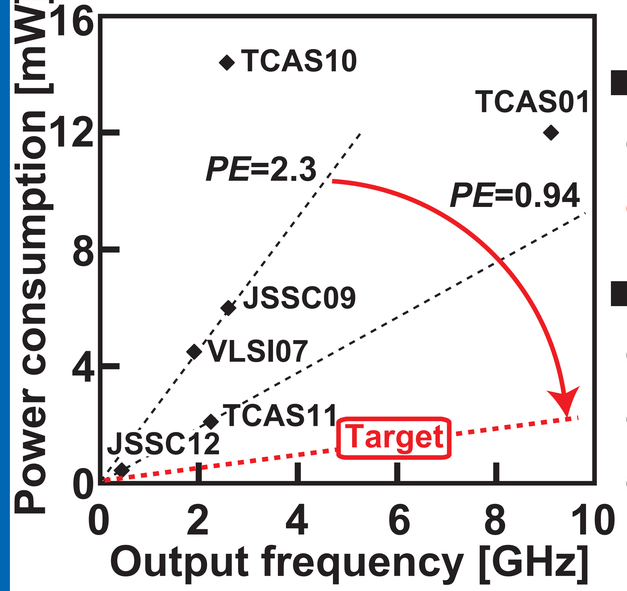
Motivation & purpose

▪Wireless Sensor Network(WSN)



● longer lifetimes and smaller volumes

Power consumption ⟵ Freq. ⟶ Antenna size

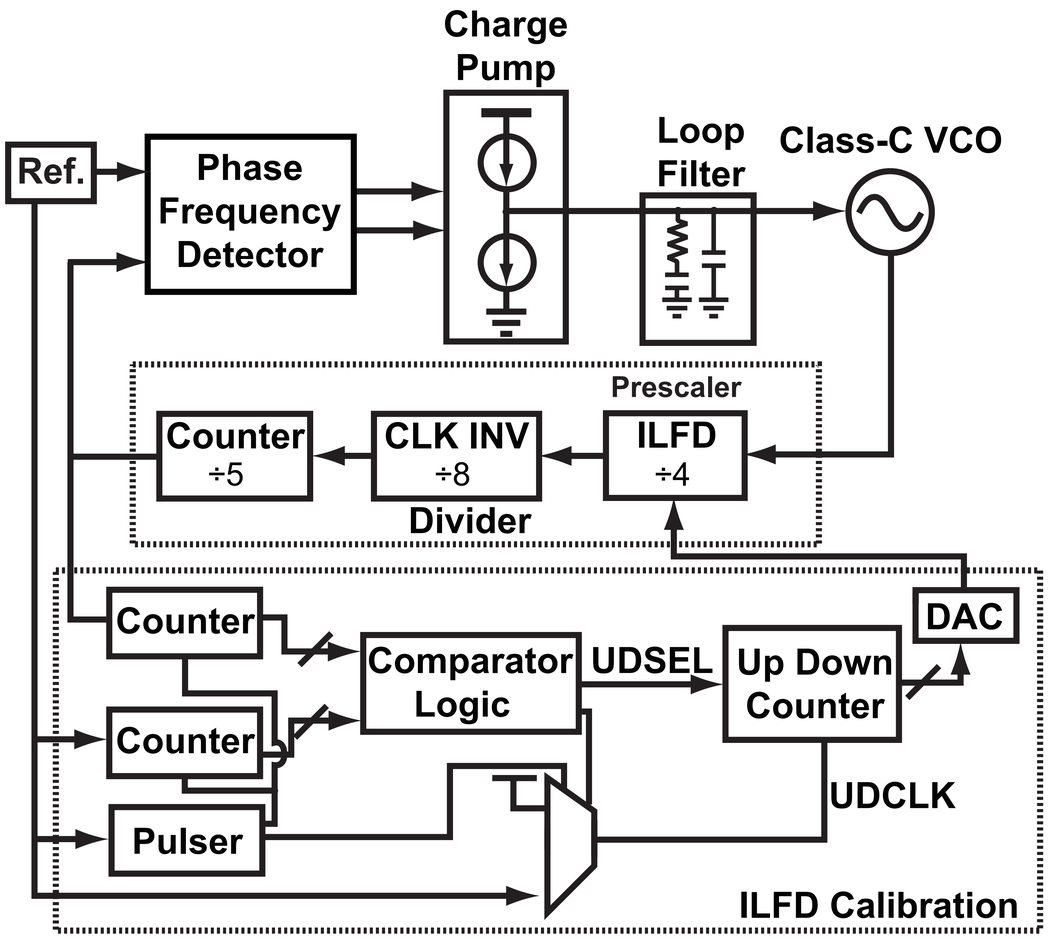


■ PLL
- ●Frequency generation
- ●Much power consumption

■ Challenge for low power
- ●low voltage for low power
- ●Frequency Divider
- ●VCO

Ultra low power PLL is required

Proposed PLL Architecture



■ ÷4 Injection locked frequency divider(ILFD)
- ●Reduce the number of divider stages
- ●Forward body bias to assist low voltage operation

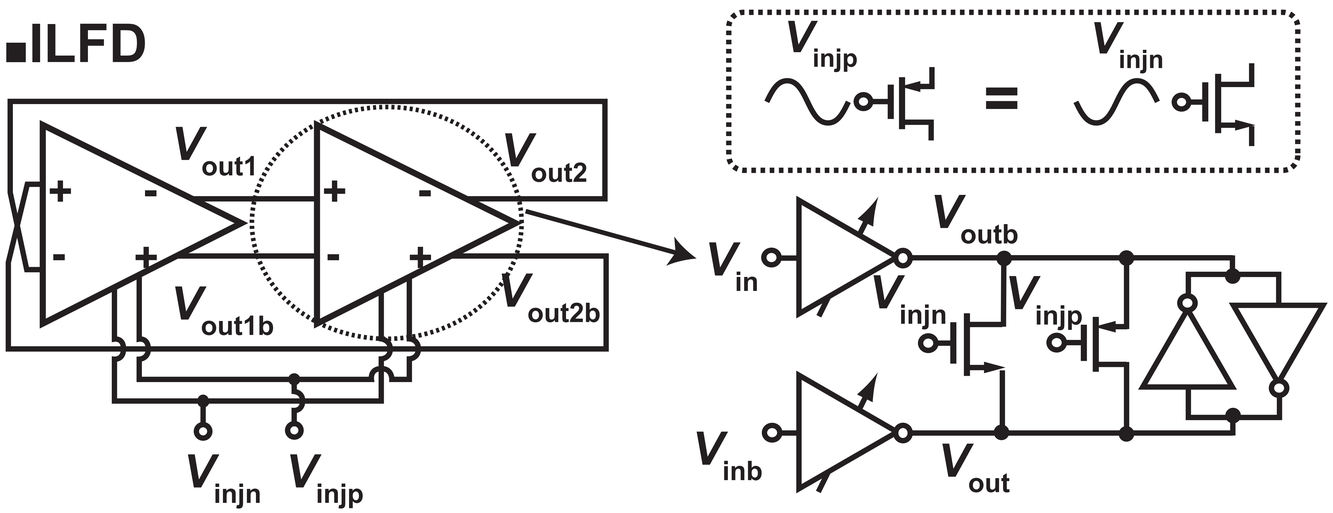
■ ILFD digital calibration
- ●control the ILFD frequency automatically.

■ Class-C VCO [1]
- ●Low power and low phase noise even in low voltage

[1] A. Mazzanti, et al., JSSC2008.

Proposed ILFD

■ILFD



■ Widen the ÷4 lock range

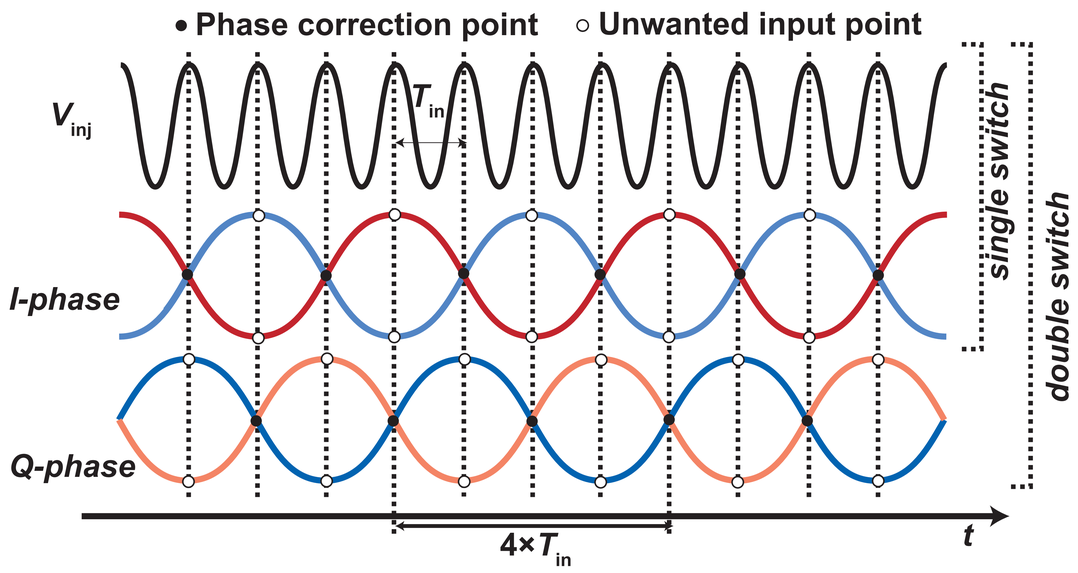
- *double switch injection* technique [2]
- Complementary input for VCO differential balance

■ Forward body bias

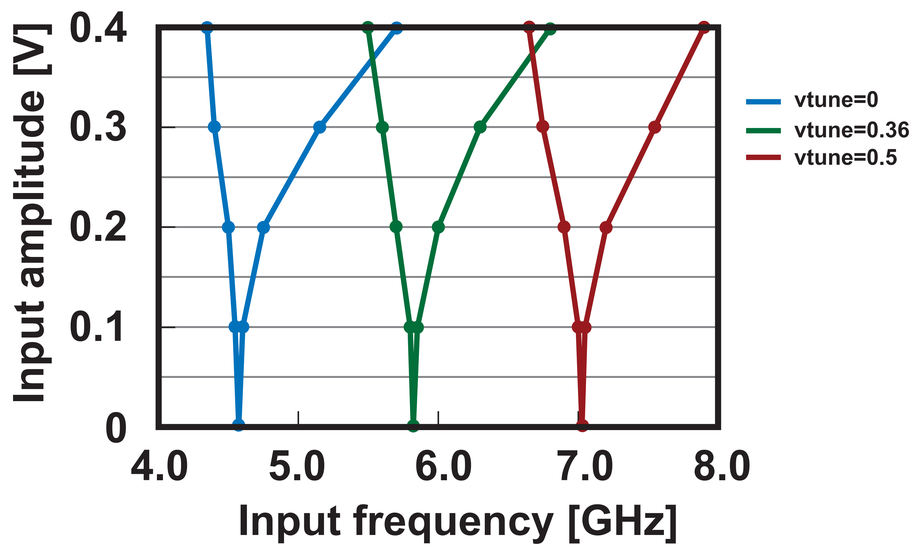
- injection switches for wide lock range
- delay cells for high operation frequency

[2] S. Ikeda, et al., ASSCC2012.

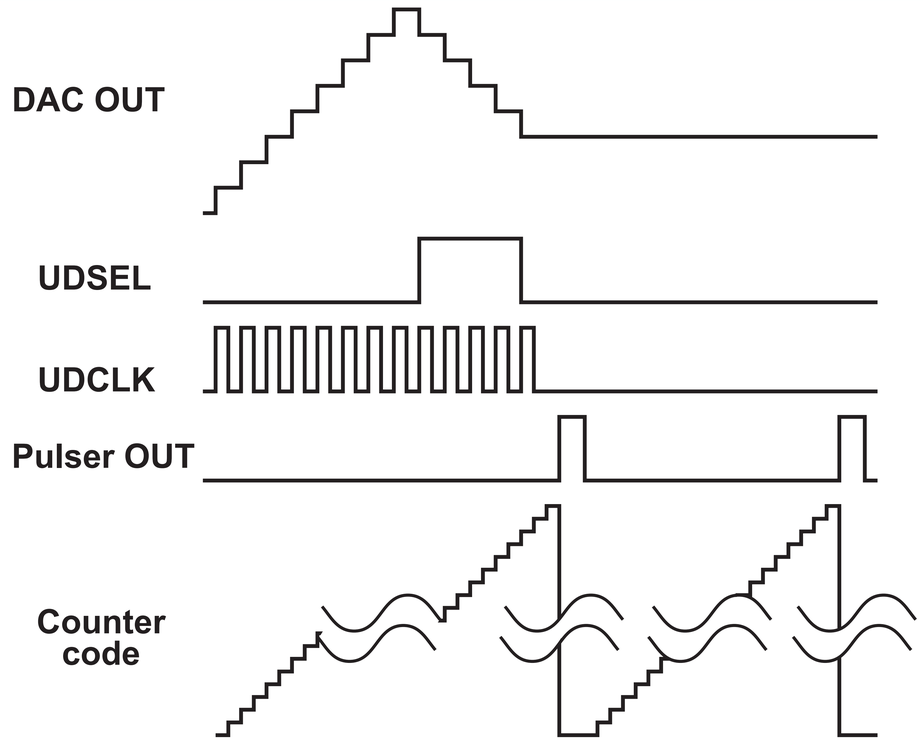
■*double switch injection technique* [2]



- Injections to peak-to-peak increase phase error.
- Phase error of 'I-phase' is compensated by phase correction of 'Q-phase' .
- Wide lock range in the case of ÷4



ILFD calibration



■ calibration mode

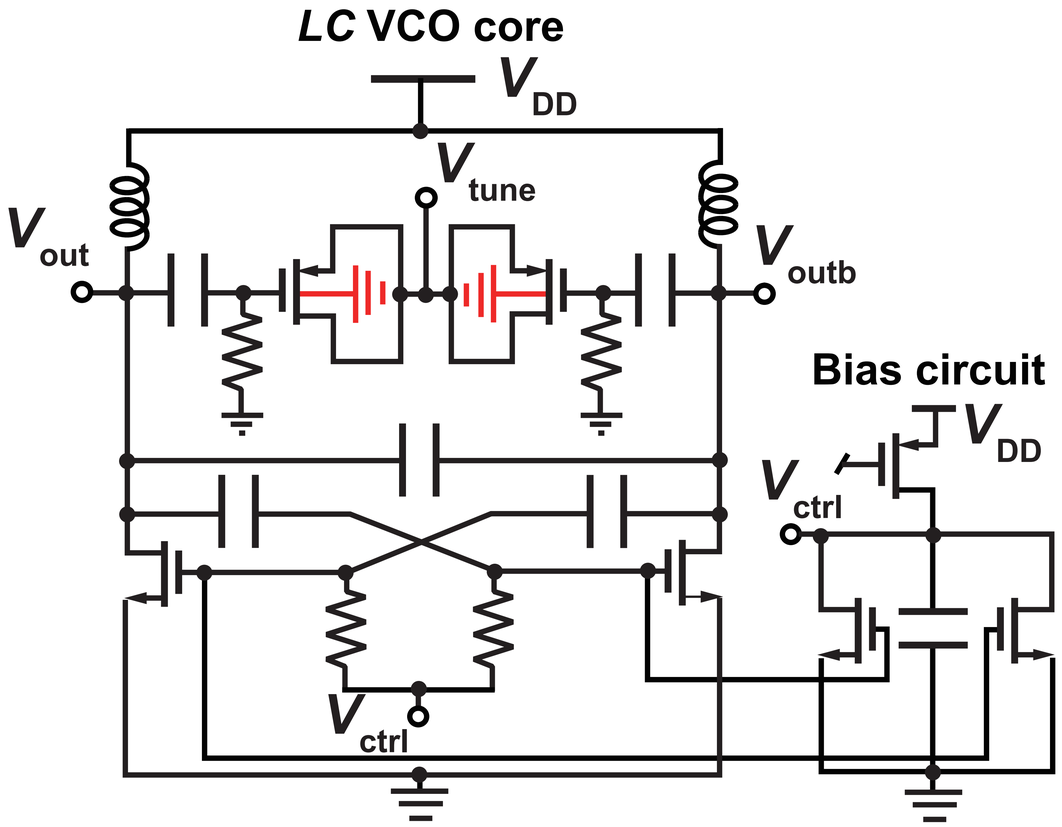
- Up down counter adjusts the code for DAC
- comparator logic control the mode of up down counter("up" or "down", UDSEL).

■ steady state

- MUX stops to supply the clock (UDCLK) for the up down counter.
- Pulser prevents the overflowing of counters.

Sho Ikeda, Tokyo Tech

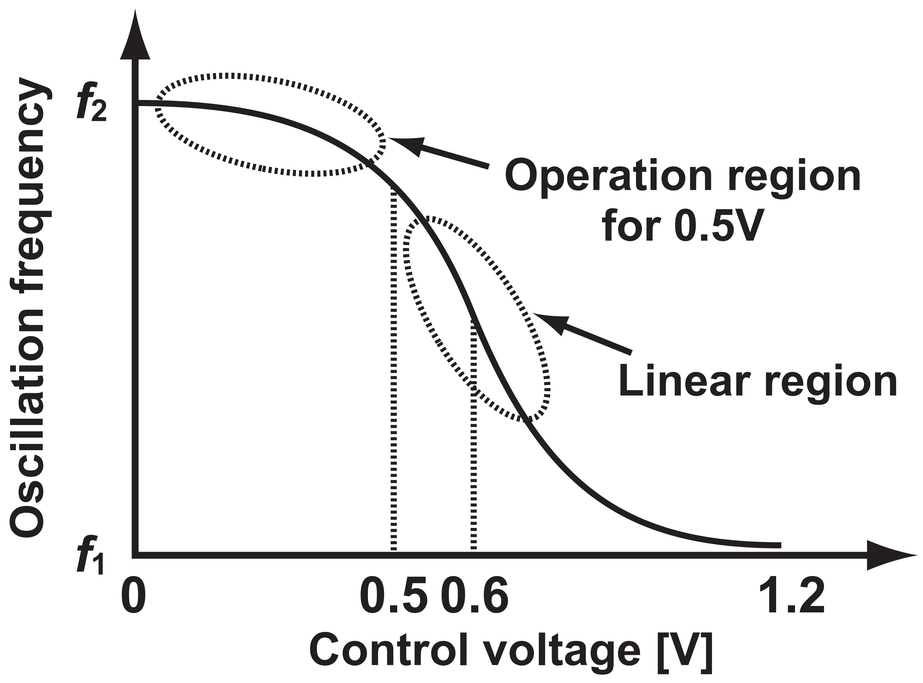
Class-C VCO

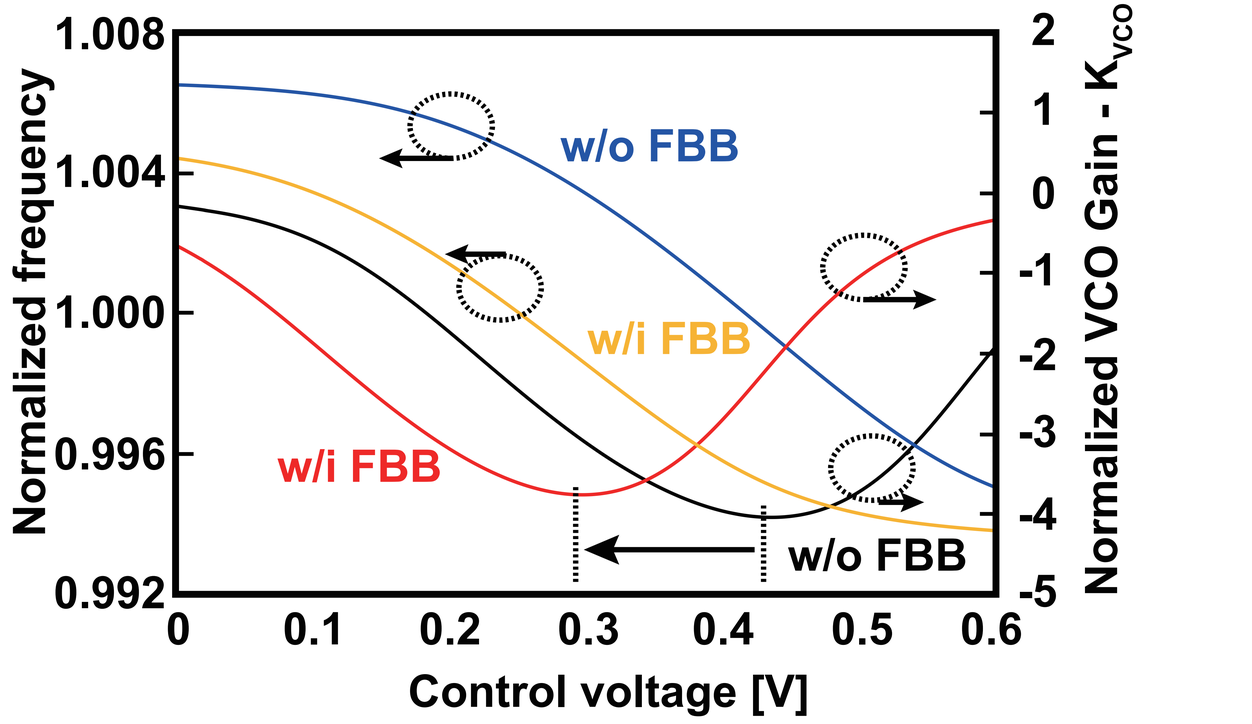


- **Class-C VCO [1]**
- **Bias circuit [3]**

[3] M. Tohidian, et al., ESSCIRC2008.

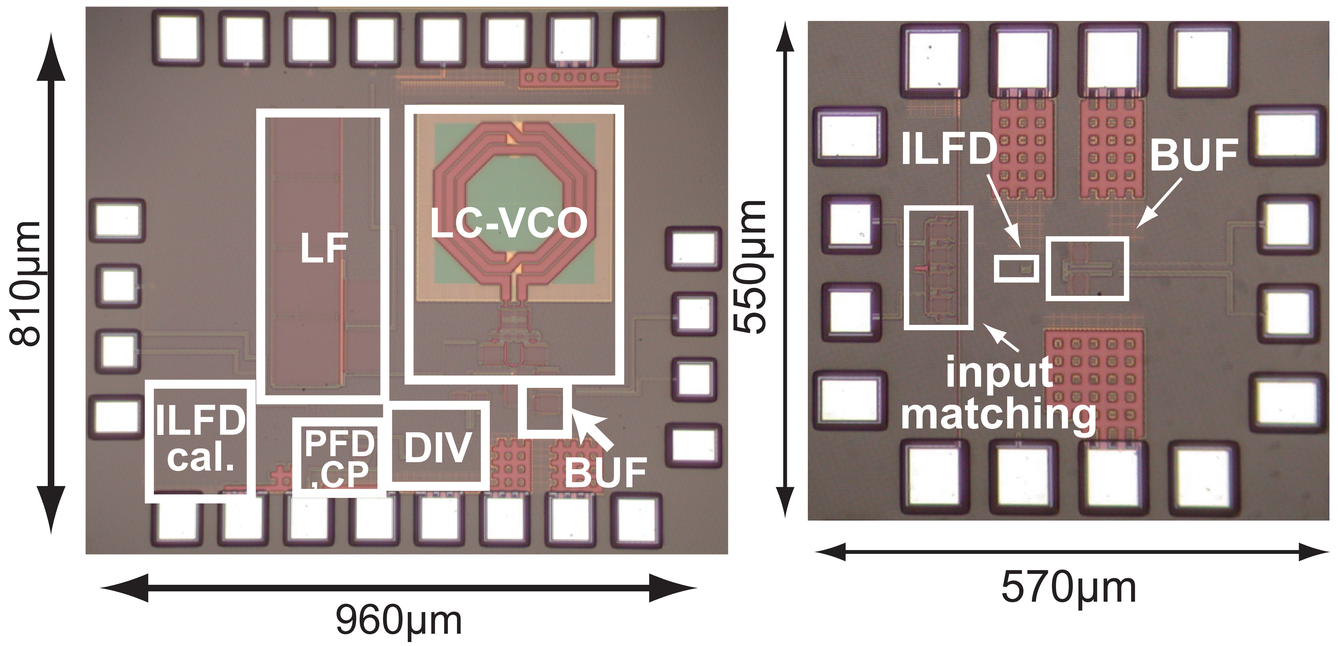
  - generate the gate bias for Class-C operation
- **FBB for varactor**
  - shift the linear region to lower control voltage





Measurement results

- **Chip photograph**

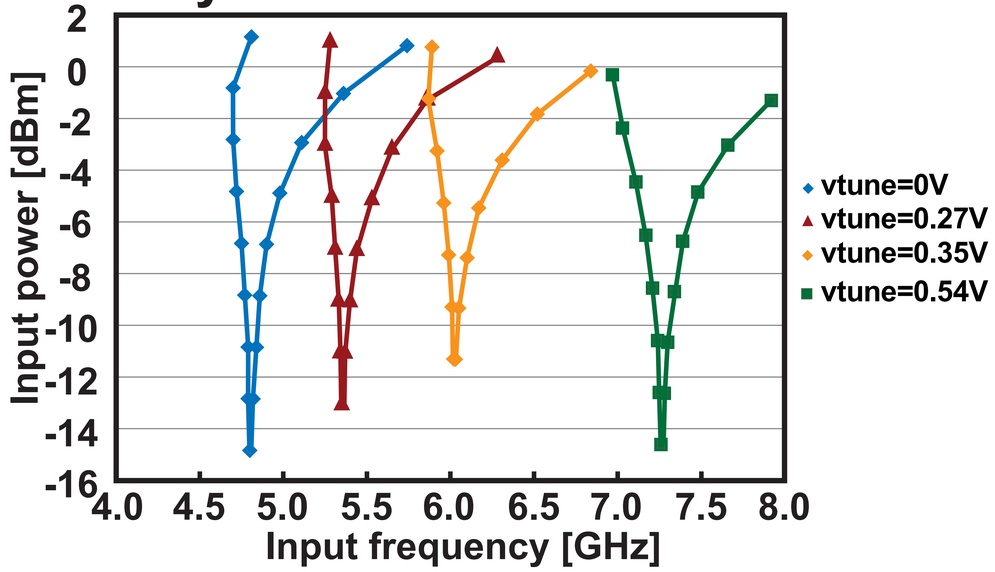


- **65nm CMOS process**
- **Low supply voltage**
  - 0.54V for divider and 0.5V for others
- **5.488 GHz output**

Sho Ikeda, Tokyo Tech

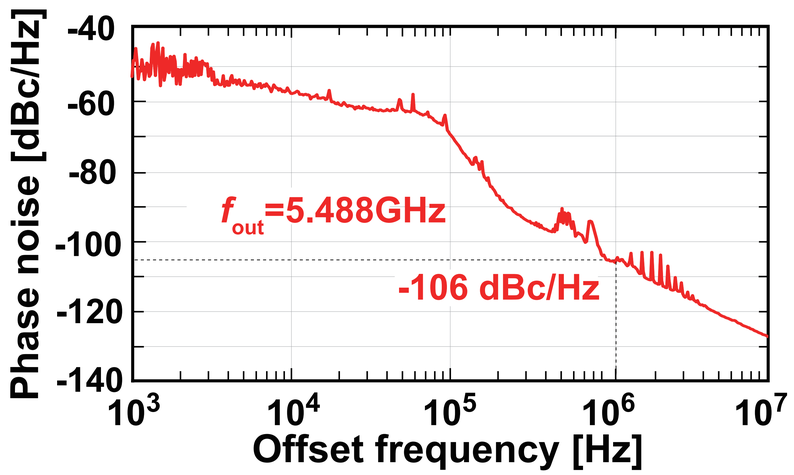
Measurement Result

■ Sensitivity Curve of ILFD



●1GHz lock range @0dBm input

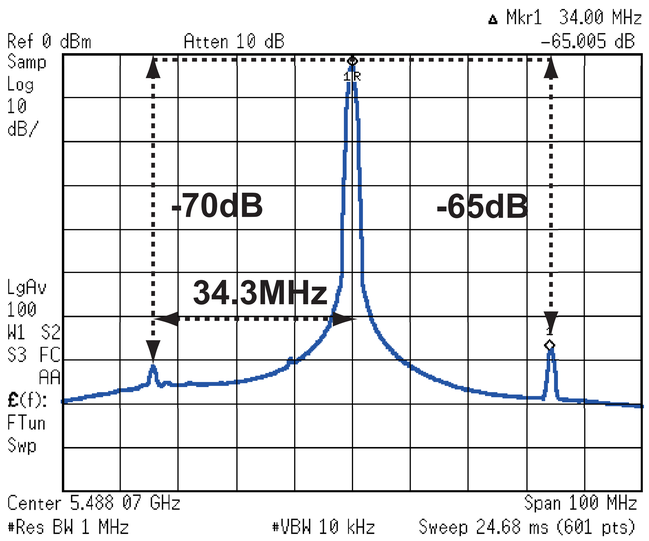
■ Phase noise



●Out-band: -106dBc/Hz@1MHz

●In-band: about -60dBc/Hz

■ Spectrum

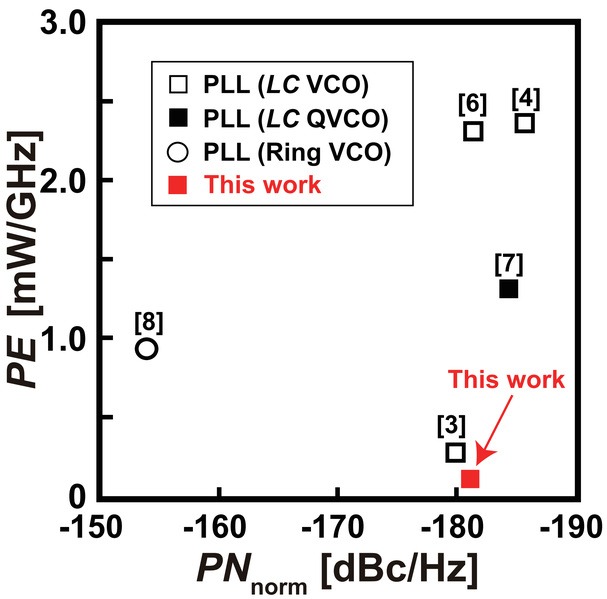


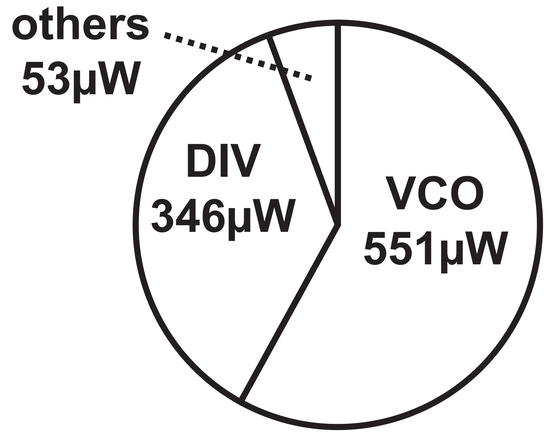
●spurious: -70dBc and -65dBc

Performance Summary

	Tech. [nm]	f_{out} [GHz]	V_{dd} [V]	PN [dBc/Hz]	Power [mW]
This work	65	5.49	0.5/0.54	-106	0.95
[4]	180	1.9	0.5	-120	4.5
[5]	180	2.56	0.5	-105	14.4
[6]	90	2.59	0.5/0.65	-113	6.0
[7]	130	9.12	0.5/0.8	-105	12
[8]	90	2.24	0.5	-87	2.1
[3]	65	5.54	0.5	-105	1.6

●Ultra low power and acceptable phase noise





[4] H.-H. Hsieh, et al., VLSI 2007
[5] C.-T. Lu, et al., TCAS 2010
[6] S.-A. Yu, et al., JSSC 2009
[7] C.-Y. Yang, et al., TCAS 2001
[8] K.-H. Cheng, et al., TCAS 2011

Conclusion

■ An ultra-low-power PLL with an ILFD and a linearized varactor under low supply voltage was proposed.

■ FBB is applied in the varactor for linearity.

■ Fabricared chip shows a great power-efficiency with acceptable phase noise under low supply voltage.

Sho Ikeda, Tokyo Tech