# An 8-ch, 20-V Output CMOS Switching Driver with 3.3-V Power Supply for Integrated MEMS Devices Controlling

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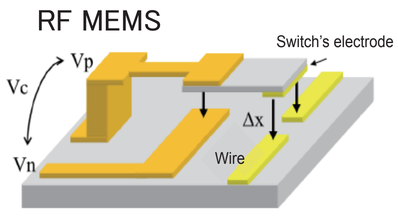
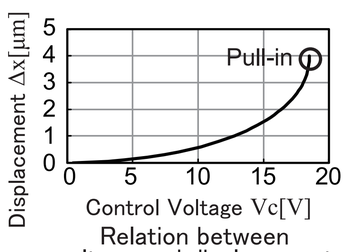
## 1. Background

### Purpose

To implement MEMS for RF devices integrating MEMS & CMOS technology




ex. MEMS switch's architecture



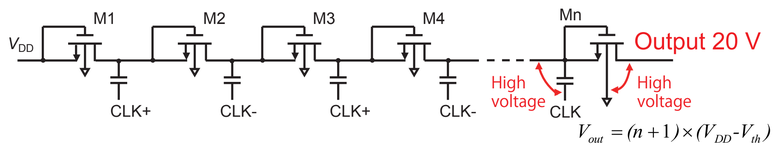

Relation between voltage and displacement

Pros
- Low loss
- Small & High performance

Cons
- Required high voltage around 20 V
- Integration of CMOS Technology

### Subject

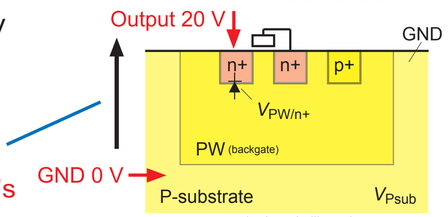
- Conventional: Dicksong type Charge pump




Breakdown voltage (180-nm CMOS)
- MIM capacitor: 5 V
- Transistor
  - PW/n+: 11 V

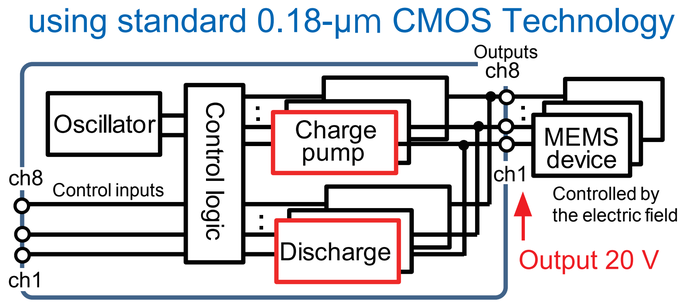
Voltage PN junction
20 V > 11 V
exceeding transistor's breakdown voltage

Section figure of twin-well nMOS transistor




### Goal

An 8-ch, 20-V Output CMOS Switching driver using standard 0.18-μm CMOS Technology

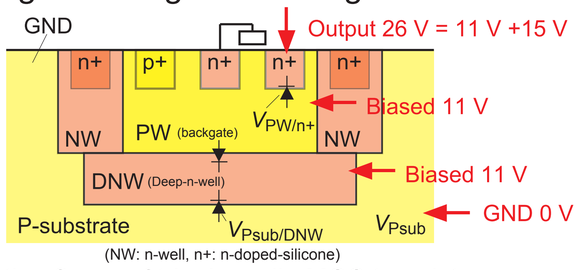



- 8-sets of charge pump, discharge circuits, oscillator and control logic circuit.
- Charge pump : Low→ High (20 V).
- Discharge circuit : High (20 V) → Low.

## 2. Proposed CMOS Switching Driver

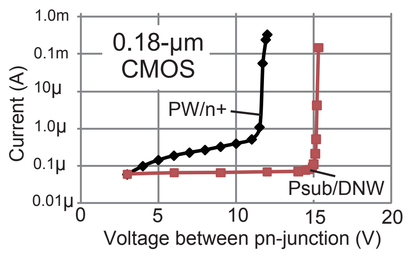
### Tripple well transistor

to get higher voltage exceeding breakdown




(NW: n-well, n+: n-doped-silicone)

Section figure of tripple-well nMOS transistor



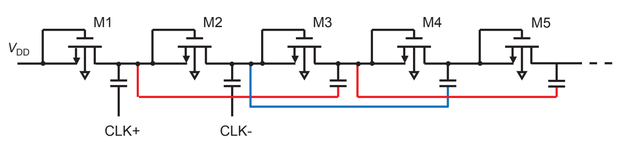

Breakdown voltage (180-nm CMOS)
- Transistor
  - PW/n+: 11 V
  - PW/DNW: 15 V
  - Psub/DNW: 15 V

Improved maximum output voltage

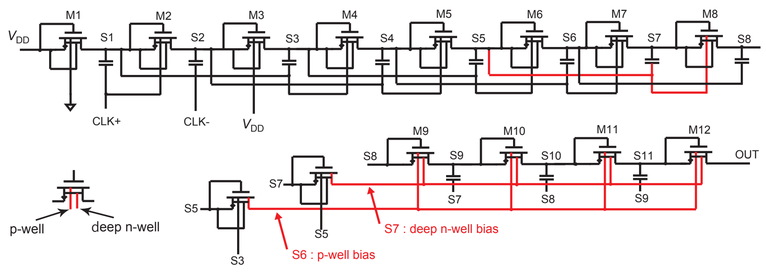
$$V_D < V_{PW/n+} + V_{Psub/DNW} = 11\text{V} + 15\text{V} = 26\text{V}$$

### Charge pump

- Proposed: Clock signal distribution technique




- Proposed: Charge pump using tripple-well transistor

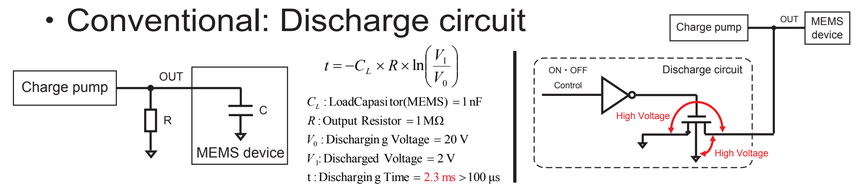



For capacitor's break down voltage
- Later stages use previous stage's signal.

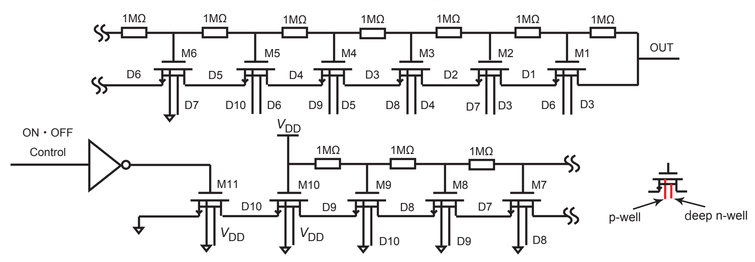
For transistor's breakdown voltage
- PW, DNW are biased by previous voltage.

### Discharge circuit

- Conventional: Discharge circuit




- Proposed: cascaded discharge circuit

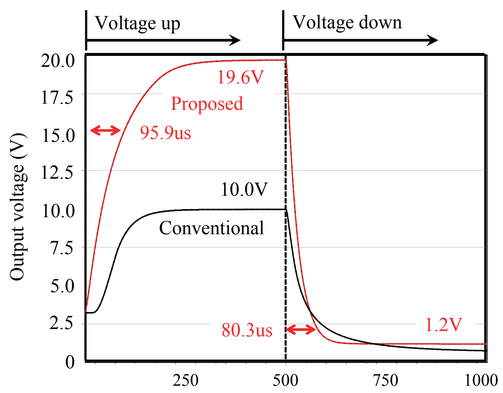



For transistor's D-S breakdown voltage
- 10-stages transistor's are cascaded.

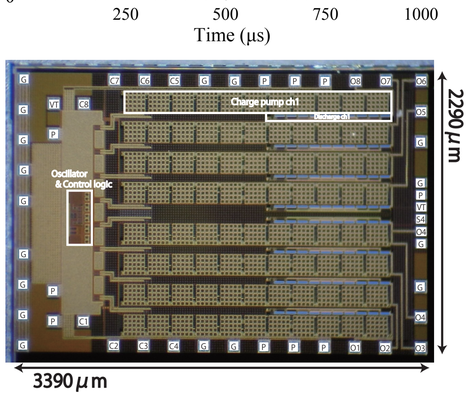
For leakage of charging current
- High resistor are used (Charge:10MΩ, Discharge:42kΩ)

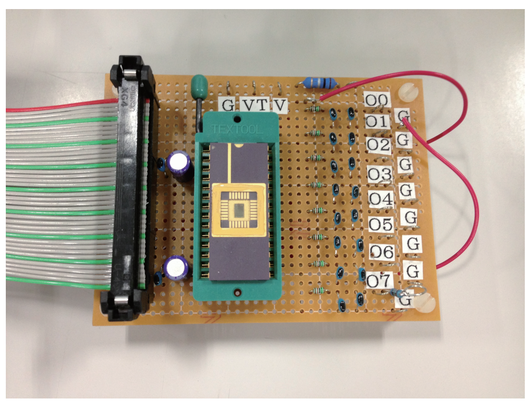
## 3. Measured Results

### Simulation & Fabricated Chip

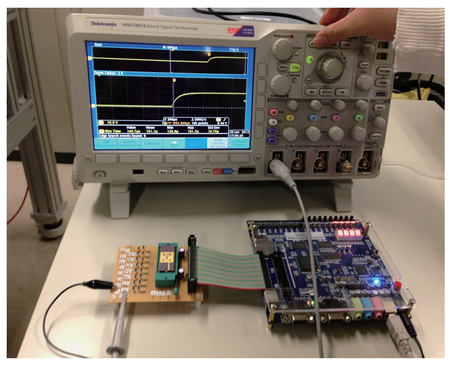


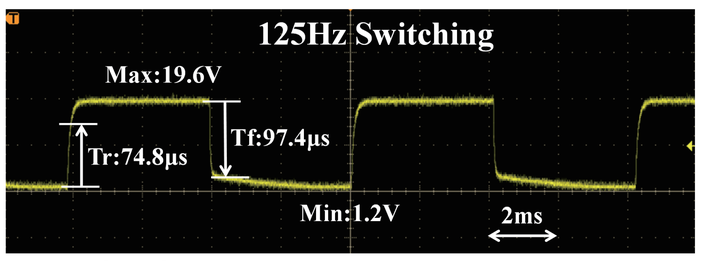

- Output voltage exceeded Tr's breakdown with 1.3-nF capacitive load
- Quick charge and discharge < 100 μs
- Fabricated by 0.18-μm CMOS process



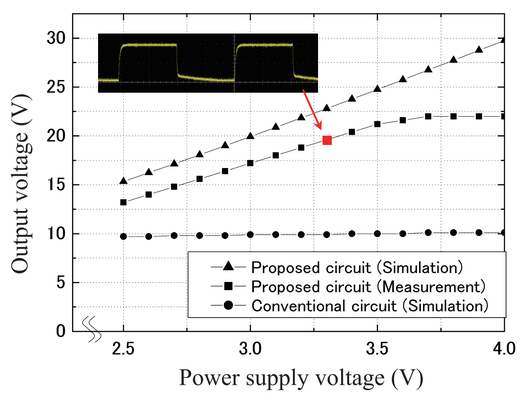




### Measurement






Confirmed 8-ch output independently




Performance summary

| Item | Goal | Measured Result |
|---|---|---|
| Output voltage (High) | 20 V | 19.6 V |
| Output voltage (Low) | 2 V | 1.2 V |
| Output channel | 8 ch | 8 ch |
| Load | 1 nF | 1.3 nF |
| Rise and fall Time | tr/tf < 100 μs | tr: 74.8 μs (15 V)<br>tf: 97.4 μs (3.3 V) |
| Power supply voltage | 3.3 V | 3.3 V |
| Power dissipation | | 85.3 mW (1 ch)<br>106 mW (8 ch) |
| Chip size | < 2400*3500 μm² | 2290*3390 μm² |
| CMOS process | 0.18 μm | 0.18 μm |

## 4. Conclusion

**An 8-ch, 20-V output CMOS switching driver with 3.3-V power supply was designed and fabricated.**

a) Confirmed 20-V output voltage exceeding 11-V transistor's breakdown voltage.

b) Tripple-well-structured n-MOS transistors were implemented in charge pump and discharging circuit.

c) Invented optimal transistor-well-biasing techniques to exceed transistor's breakdown voltage.