A 950μW 5.5-GHz Low Voltage PLL with Digitally-Calibrated ILFD and Linearized Varactor

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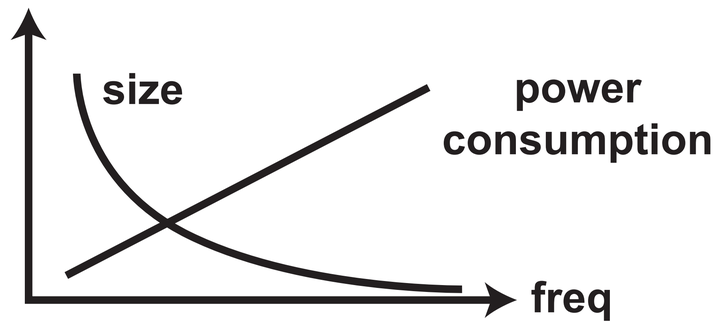
Motivation & Purpose

■ **Wireless Sensor Network(WSN)**

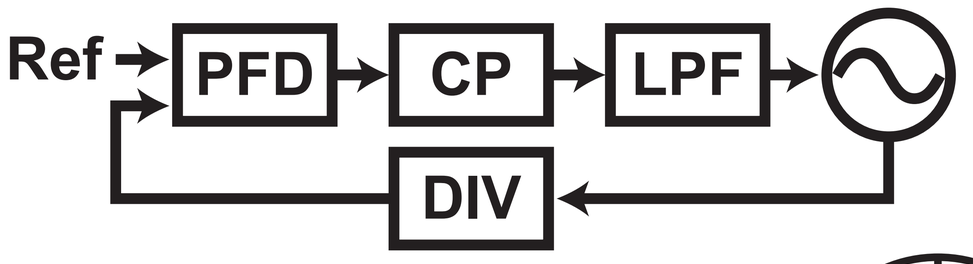
req. :longer lifetimes, smaller volumes



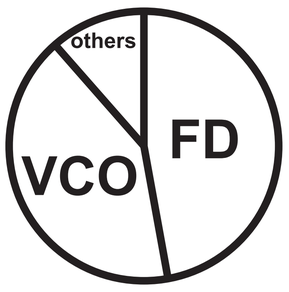
Power consumption ∝ f ← Freq. → Antenna size ∝ $1/f$

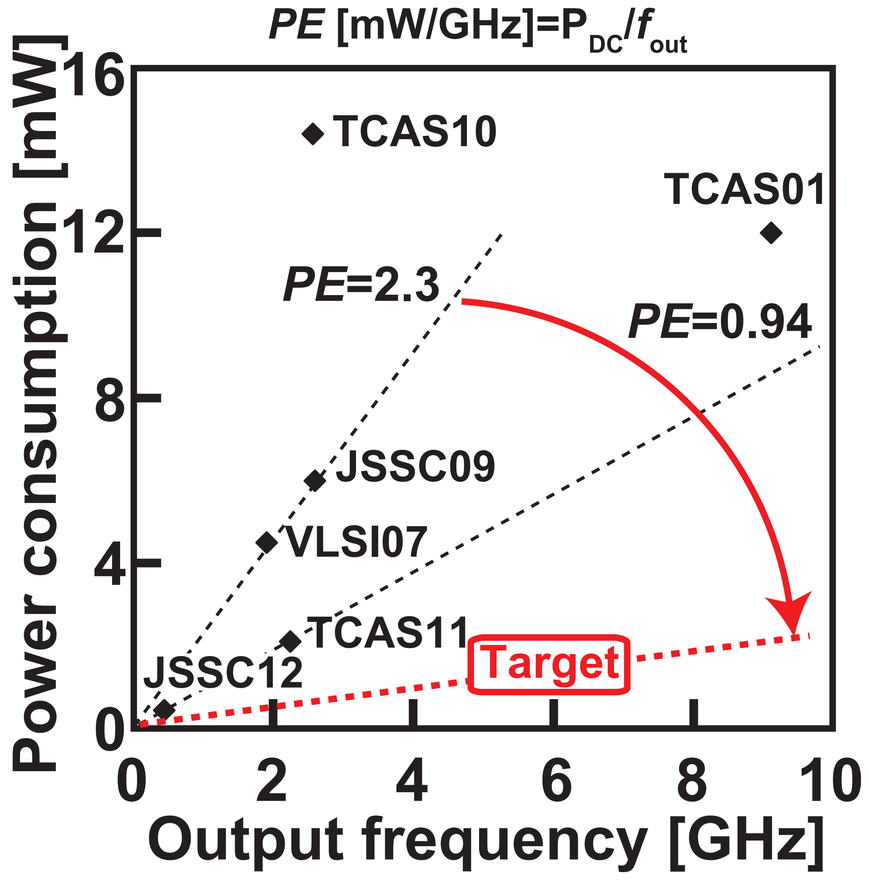
- High power consumption in high freq. RF circuits
- Small size antenna in high freq.
- Low gain in small size antenna

■ **Phase locked loop (PLL)**



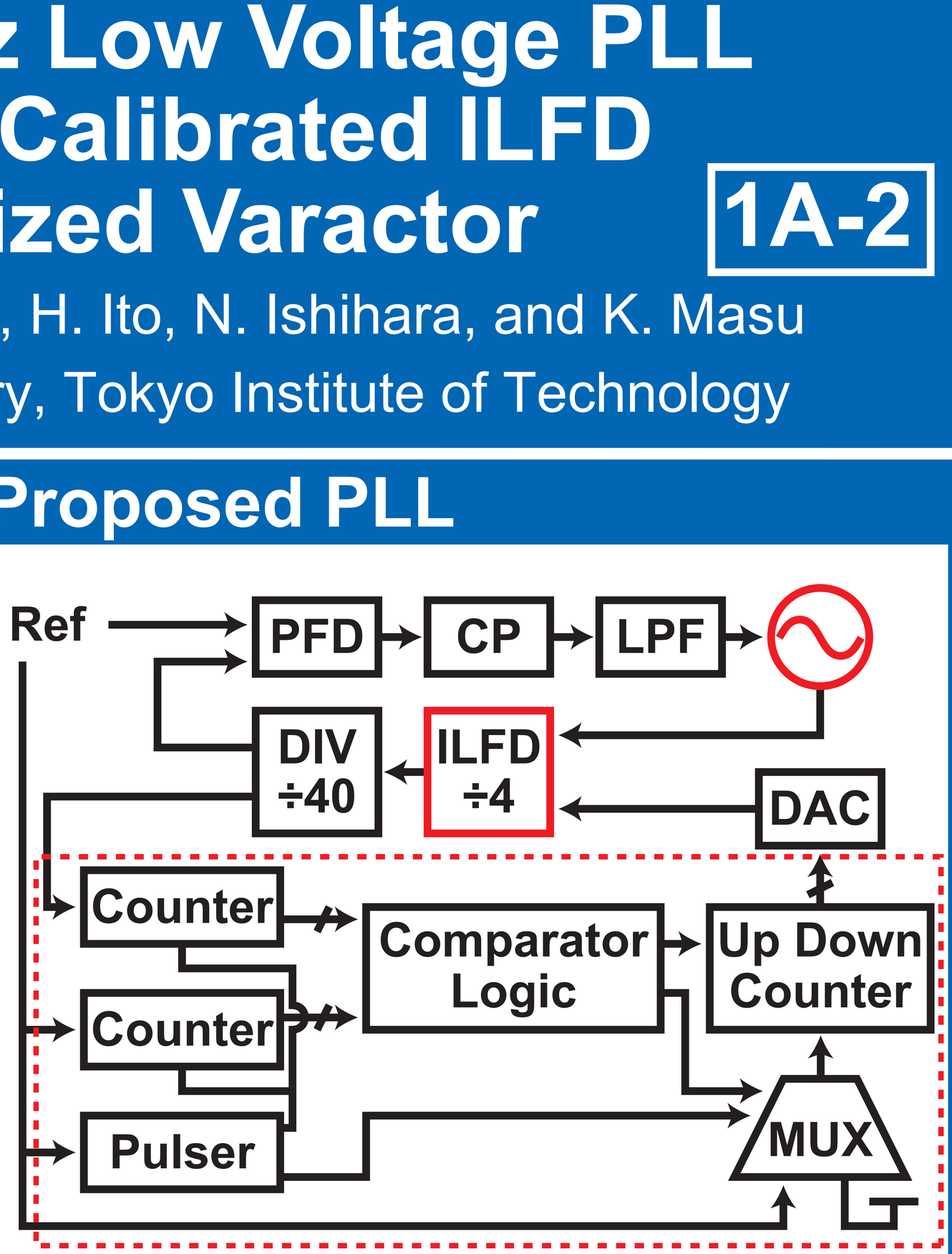
- Challenge for low power
  - Frequency Divider (FD)
  - VCO





Ultra low power PLL is required

Proposed PLL

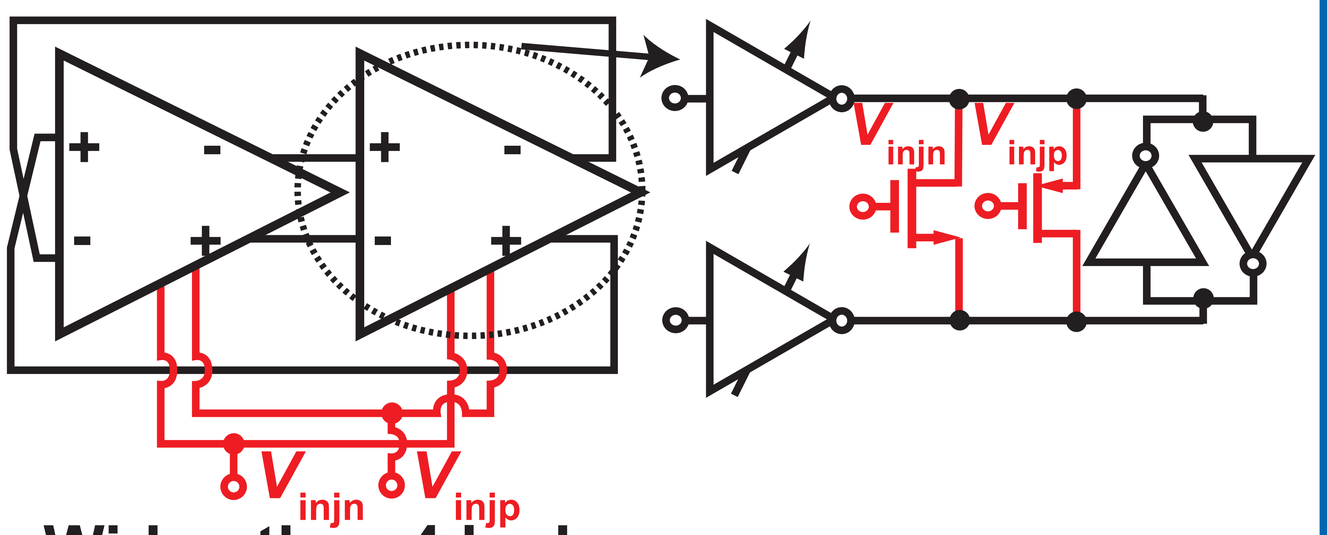


- ÷4 Injection locked frequency divider
  - Reduce the number of divider stages
  - Forward body bias for low voltage
- ILFD digital calibration
  - control the ILFD frequency automatically.
- Class-C VCO [1]
  - Low power and low phase noise even in low voltage

[1] A. Mazzanti, et al., JSSC2008.

Circuit detail

■ **Injection locked frequency divider (ILFD)**



- Widen the ÷4 lock range
  - *double switch injection* technique [2]
- Forward body bias (FBB) for low voltage
  - injection switches for wide lock range
  - delay cells for high operation frequency

[2] S. Ikeda, et al., ASSCC2012.