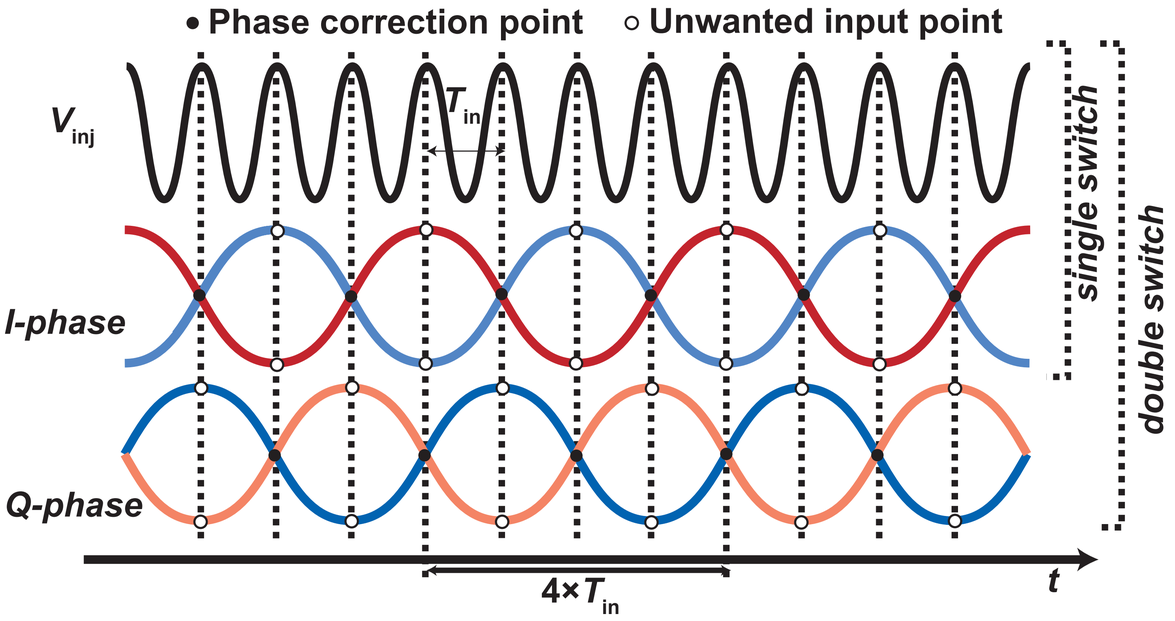
■*Double switch injection technique* [2]

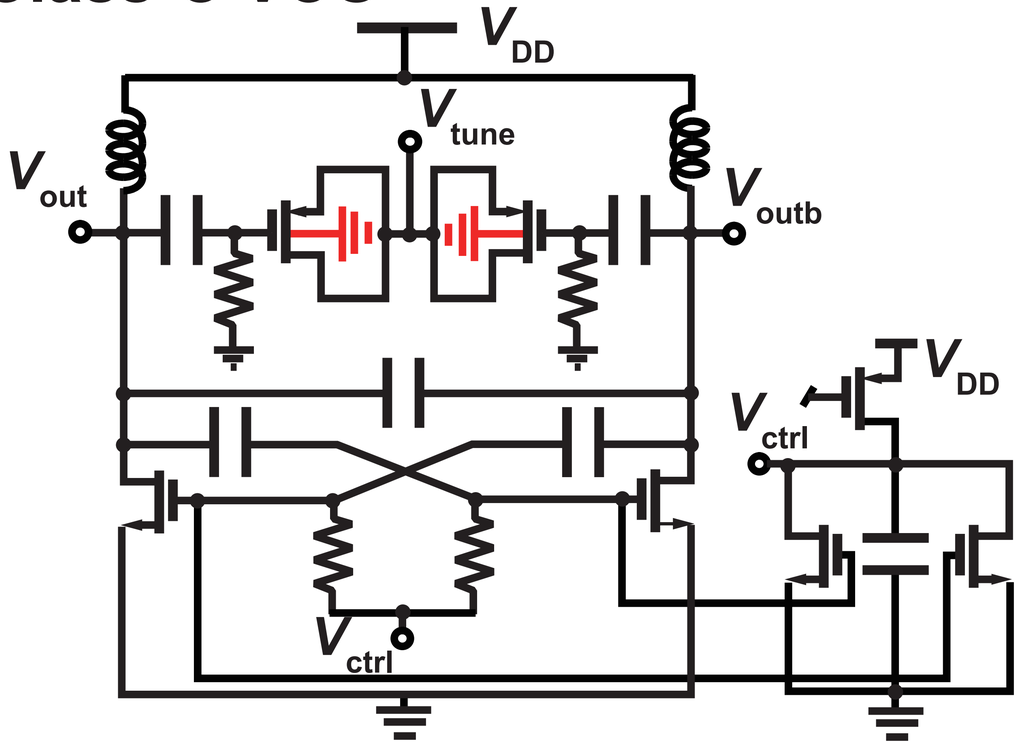


- Injections to peak-to-peak increase phase error.
- Phase error of 'I-phase' is compensated by phase correction of 'Q-phase' .
- Wide lock range in the case of ÷4

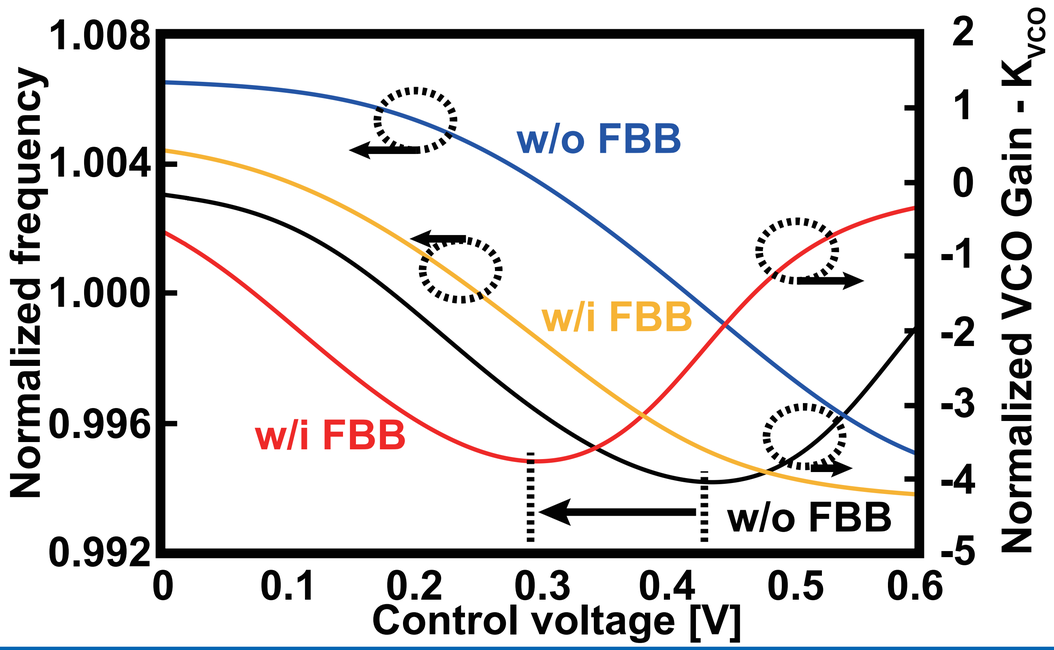
■FLL(Frequency Locked Loop) for ILFD digital calibration

- calibration mode
  - Up down counter adjusts the code for DAC
  - comparator logic control the mode of up down counter("up" or "down", UDSEL).
- steady state
  - MUX stops to supply the clock (UDCLK) for the up down counter.
  - Pulser prevents the overflowing of counters.

■Class-C VCO

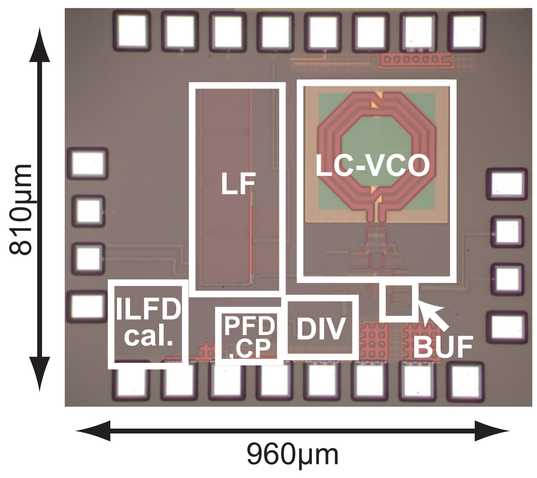


- Class-C VCO [1]
- Bias circuit [3] [3] M. Tohidian, et al., ESSCIRC2008.
  - gate bias for Class-C operation
- FBB for varactor
  - shift the linear region to lower voltage



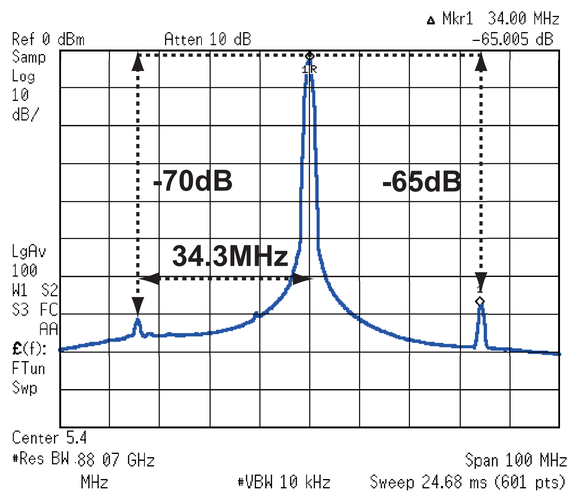
Measurement Result

■Chip micropraph

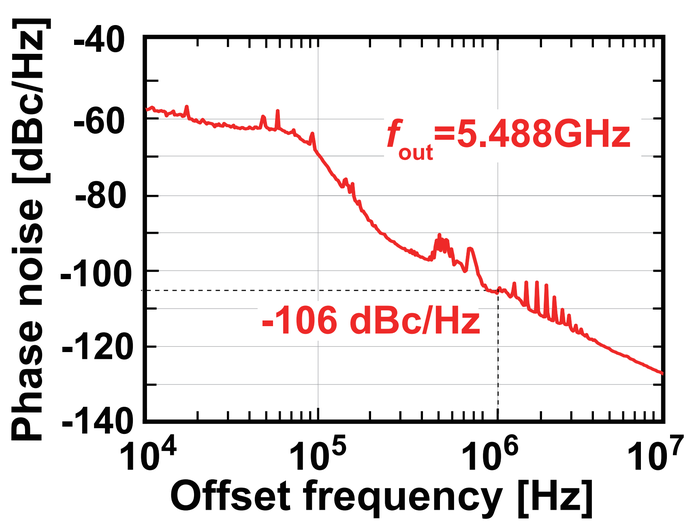


- 65nm CMOS
- Low supply voltage
  - 0.5V : others
  - 0.54V : divider
- Output frequnecy
  - 5.488 GHz

■Output spectrum & phase noise



- spurious: -70dBc and -65dBc

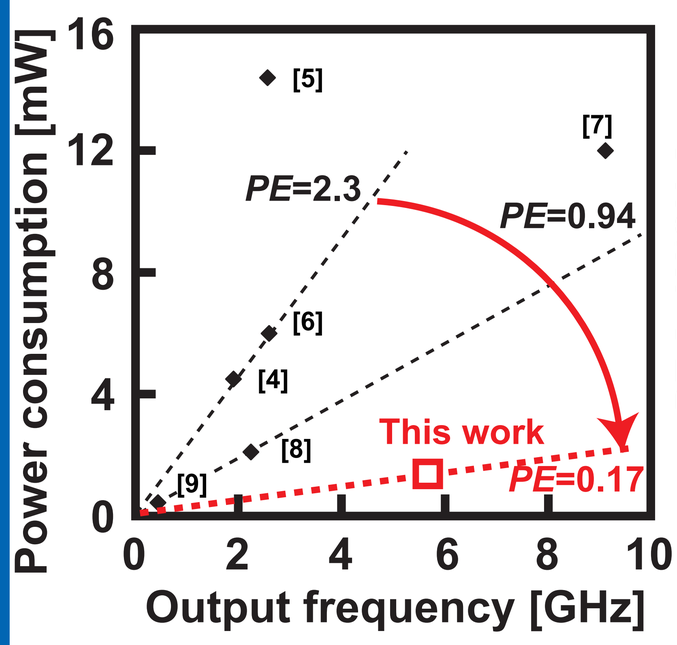


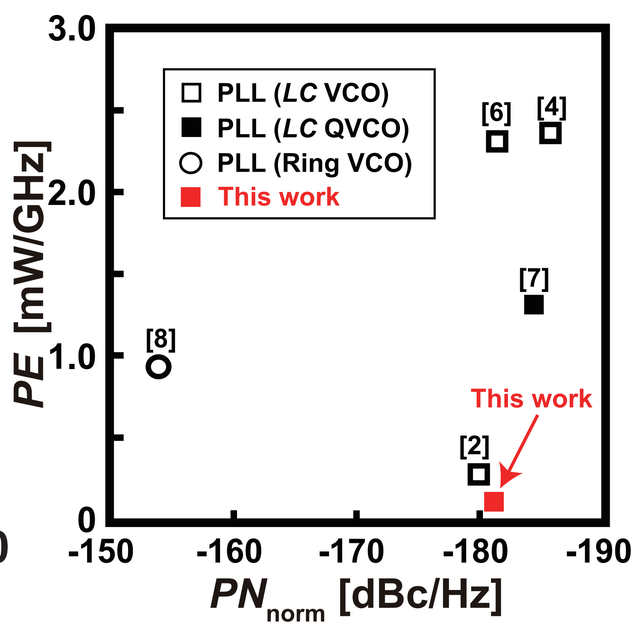
- Out-band: -106dBc/Hz@1MHz
- In-band: about -60dBc/Hz

■Performance summary and comparison

	Tech. [nm]	f_{out} [GHz]	V_{dd} [V]	PN [dBc/Hz]	Power [mW]
This work	65	5.49	0.5/0.54	-106	0.95
[4]	180	1.9	0.5	-120	4.5
[5]	180	2.56	0.5	-105	14.4
[6]	90	2.59	0.5/0.65	-113	6.0
[7]	130	9.12	0.5/0.8	-105	12
[8]	90	2.24	0.5	-87	2.1
[2]	65	5.54	0.5	-105	1.6

- Ultra low power and acceptable phase noise





[4] H.-H. Hsieh, et al., VLSI 2007
[5] C.-T. Lu, et al., TCAS 2010
[6] S.-A. Yu, et al., JSSC 2009
[7] C.-Y. Yang, et al., TCAS 2001
[8] K.-H. Cheng, et al., TCAS 2011
[9] W.-H. Chen, et al., JSSC 2012

Conclusion

- An ultra-low-power low voltage PLL
  - · Class-C VCO · divide-by-4 ILFD
  - · Linear varactor under low voltage
- 5.5GHz, 0.95mW

→great power-efficiency:0.17mW/GHz

Sho Ikeda, Tokyo Tech