A 0.5-V 5.8-GHz Current-Reuse-VCO-Based PLL with Amplitude Regulation Technique

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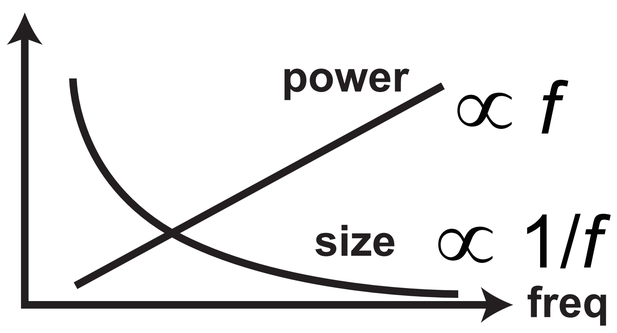
Motivation & Purpose

■**Wireless Sensor Network(WSN)**

req. :longer lifetimes, smaller volumes



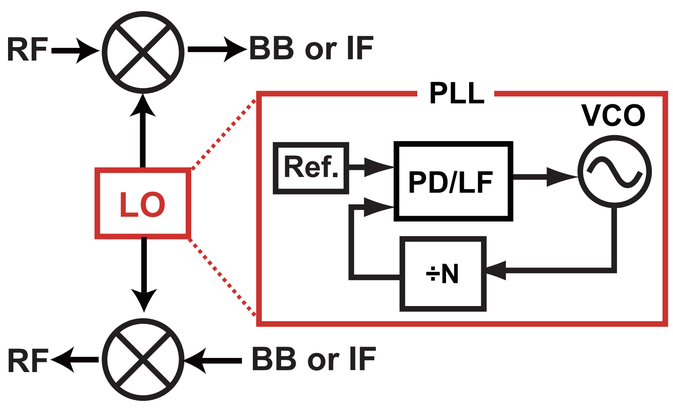
Power consumption

Freq.

Antenna size

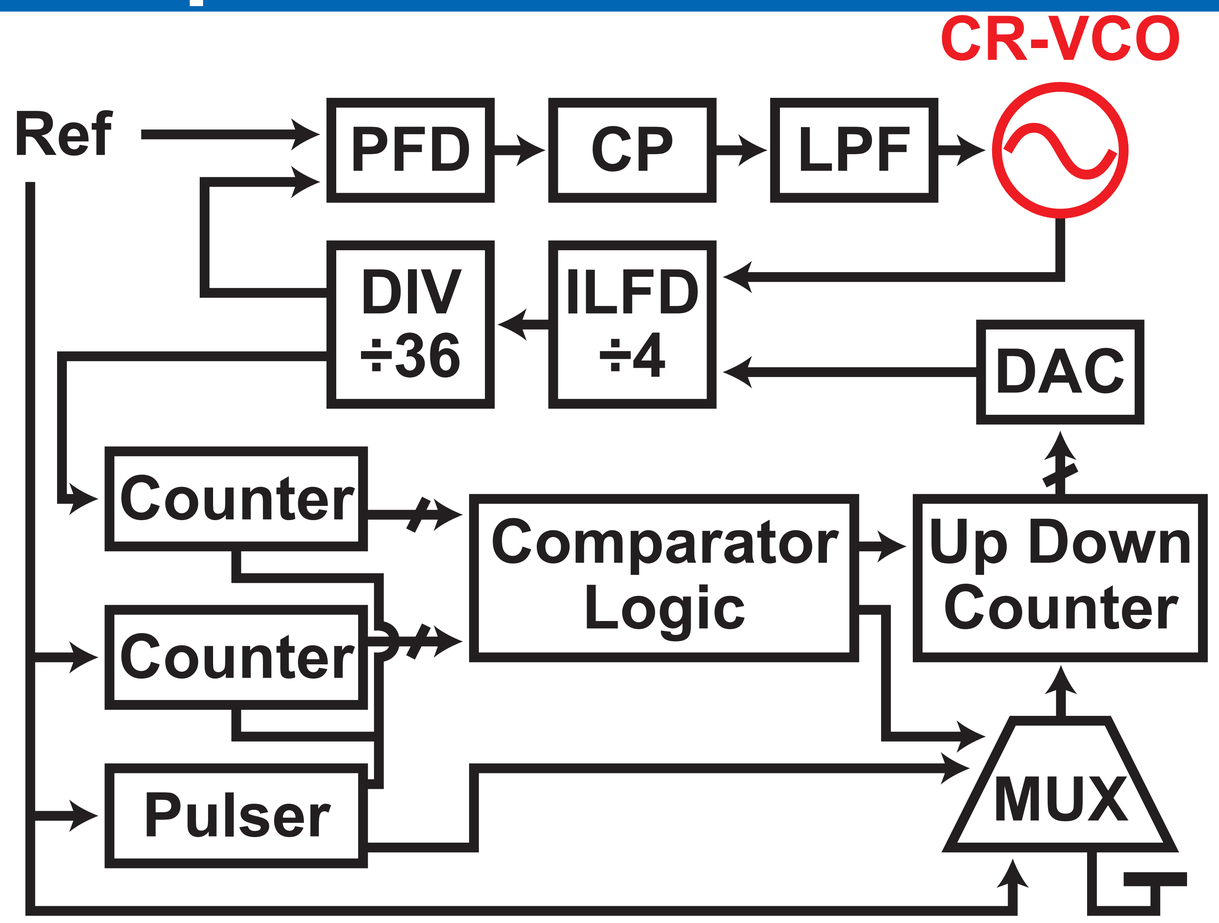
■**Phase-locked loop (PLL)**

- **Much power consumption in RF transceiver (especially in high frequency)**



Ultra low power PLL is required

Proposed PLL



■ **0.5V supply voltage**

- **Reduce power consumption of all over system**

■ **Current-reuse VCO [1]**

- **Low power consumption**

■ **÷4 Injection-locked frequency divider (ILFD)**

- **relax requirements of first stage divider**

■ **ILFD digital calibration**

- **cover PVT variations under low voltage.**

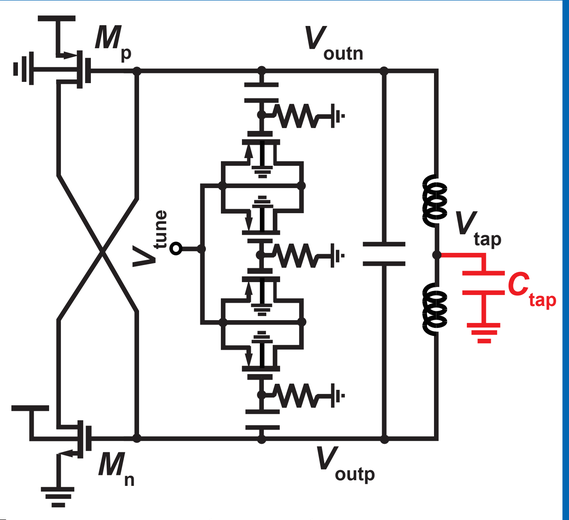
[1]S.-J. Yun, et al, ISSCC2005

Proposed amplitude regulation technique

■ **Current-reuse VCO**

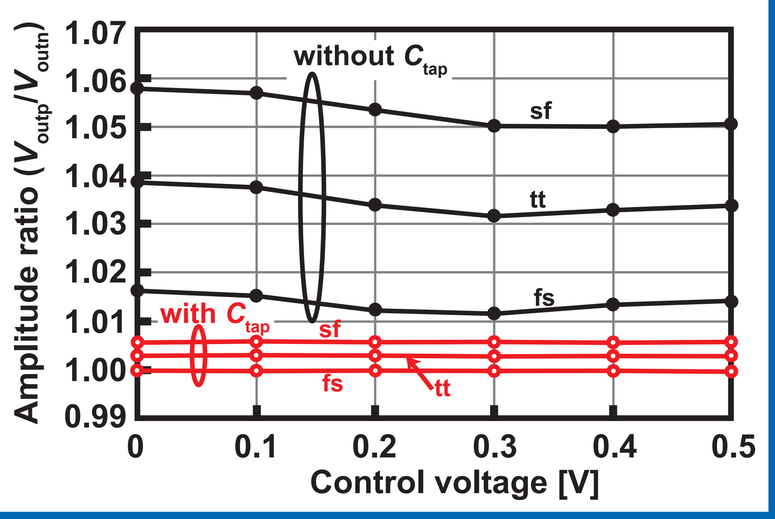
☺ **Low power consumption**

☹ **amplitude-mismatch due to its asymetric structure**

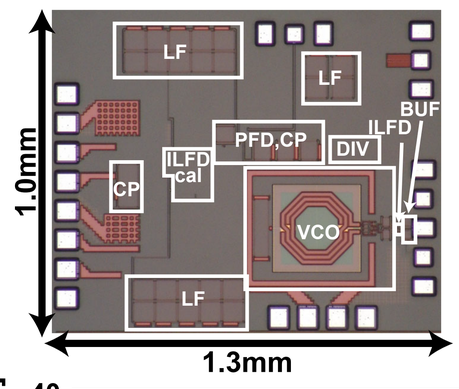


■ **Large capacitor at the center tap**

- **shunted to AC gnd**
- **amplitude-mismatch is minimized.**



Measurement results

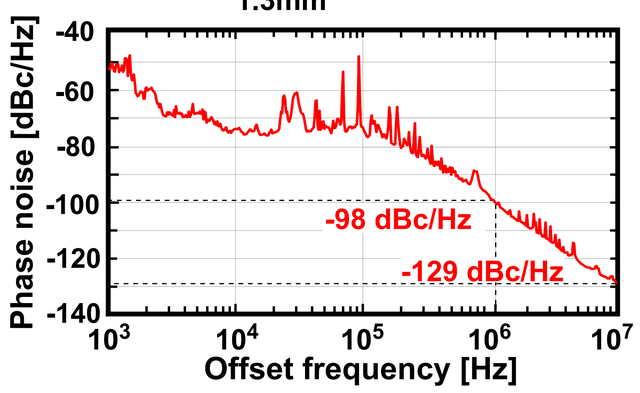


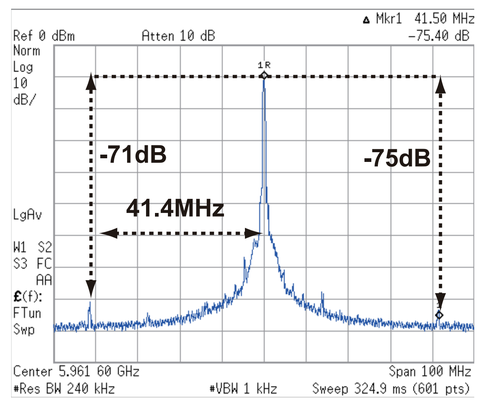
■ **65nm CMOS**

■ **0.5V supply voltage**

■ **5.96GHz output**

■ **690μW**





PE[mW/GHz]=P_{DC}/f_{out}

$PN_{norm}=PN-20\log(f_{out}/f_{offset})$

	Tech. [nm]	f_{out} [GHz]	V_{DD} [V]	PN [dBc/Hz]	Power [mW]
This	65	5.96	0.5	-129@10MHz	0.69
VLSI07	180	1.9	0.5	-120@1MHz	4.5
JSSC09	90	2.59	0.5/ 0.65	-113@1MHz	6.0
TCAS01	130	9.12	0.5/ 0.8	-105@1MHz	12
TCAS11	90	2.24	0.5	-87@1MHz	2.1
VLSI04	90	5.0	0.6 -1.2	-115@1MHz	10

Conclusion

■ **0.5V PLL with amplitude-regulated current-reuse VCO and ILFD**

■ **690μW, 5.96GHz, -129dBc/Hz@10MHz**