Ultra-Low-Power RF CMOS Transceiver Design

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Motivation: Ultra-Low-Power RF Circuit

Wireless Sensor Network (WSN)

- The significant challenges are minimization of the sensor device cost.

e.g. Battery-less sensor device
- Ultra-low-power RF
- Energy harvesting (EH) ...

Low Supply Voltage Operation

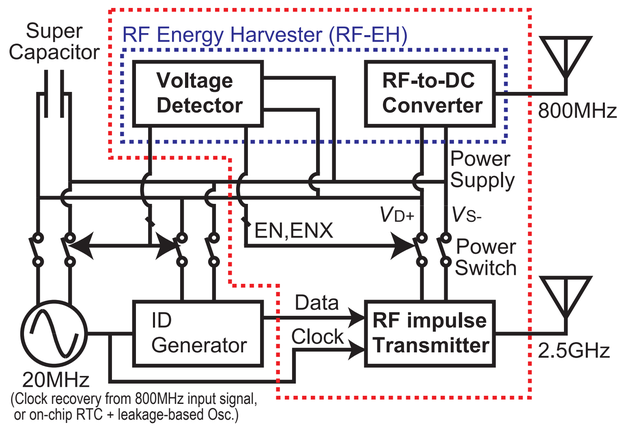
☺ Low power consumption
☹ Low signal-to-noise-ratio (SNR)
☹ Low operational freqency
☹ Low voltage headroom

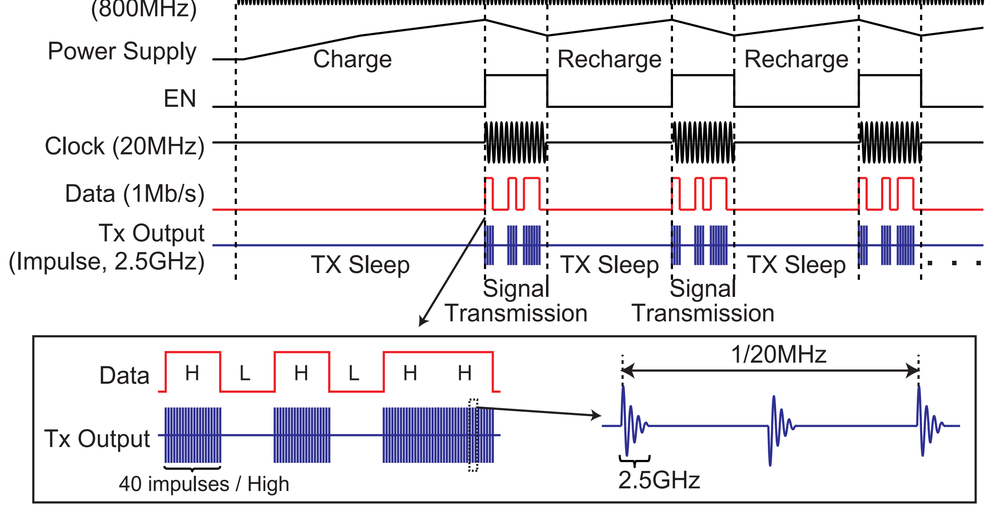
Target: Ultra-low-power transceiver with low supply voltage operation

Impulse OOK Transmitter with RF Energy harvester[1]

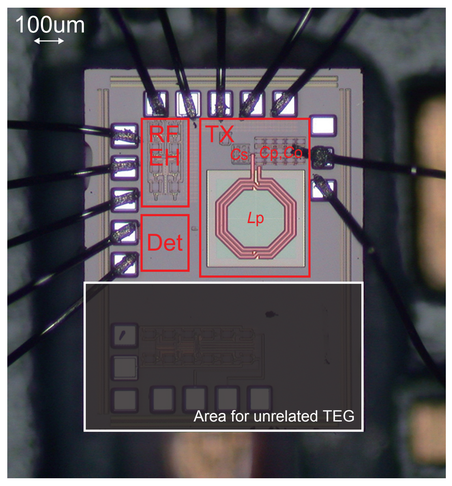
[1] H. Ito et al., RFIC, pp. 13-15, 2014

System Architecture





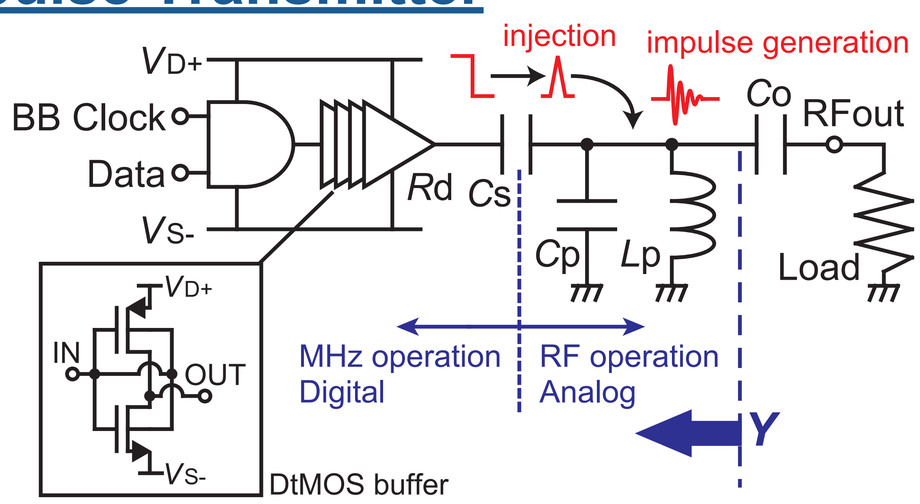
Operation



Fabricated in 65-nm CMOS

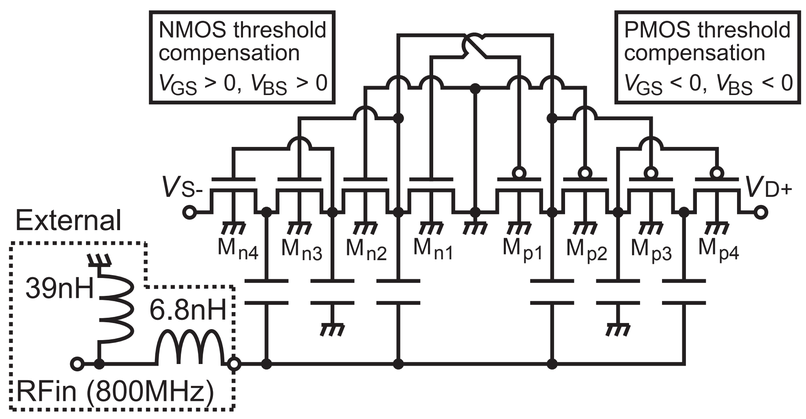
- Simplification of power management
  - LDO-less, powered by directly by RF-EH

Impulse Transmitter



- Maximally digital architecture
  - Ultra-low power and superior energy per bit

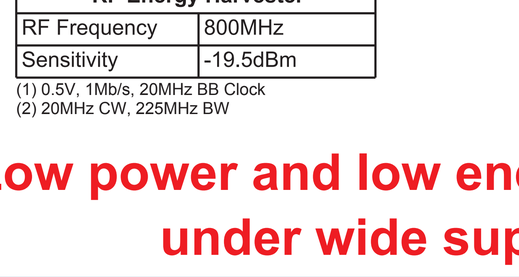
Dickson-type RF Energy Harvester



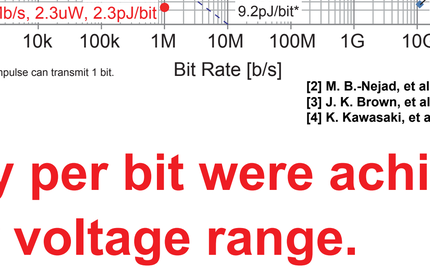
- Threshold compensation
  - High conversion efficiency and sensitivity

Measurement Results

TX frequency characteristics

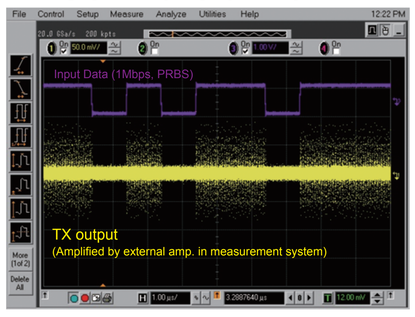


TX output waveform



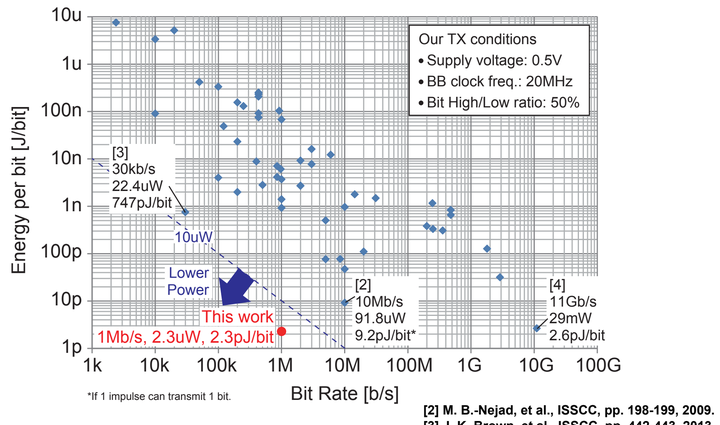
RF-EH performance

OOK waveform of TX



Technology	65nm CMOS
Die Area	680um X 560um
TX only	
Supply Voltage	0.4 - 1.0V
Modulation	OOK
Carrier Freq.	2.47GHz
Power (1)	2.3uW
Energy per bit (1)	2.3pJ/bit
Output Power (2)	-62.1dBm
RF Energy Harvester	
RF Frequency	800MHz
Sensitivity	-19.5dBm

(1) 0.5V, 1Mb/s, 20MHz BB Clock
(2) 20MHz CW, 225MHz BW



[2] M. B.-Nejad, et al., ISSCC, pp. 198-199, 2009.
[3] J. K. Brown, et al., ISSCC, pp. 442-443, 2013.
[4] K. Kawasaki, et al., ISSCC. pp. 414-415, 2010.

Low power and low energy per bit were achieved under wide supply voltage range.