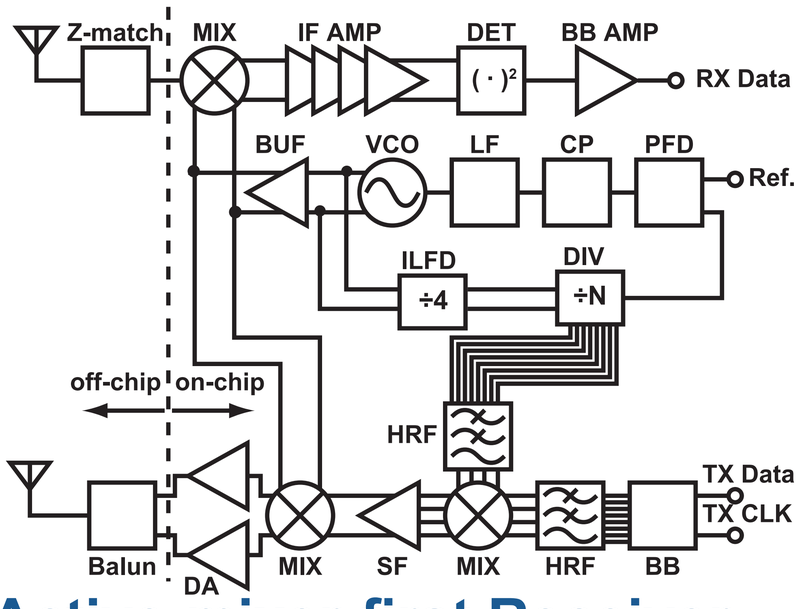
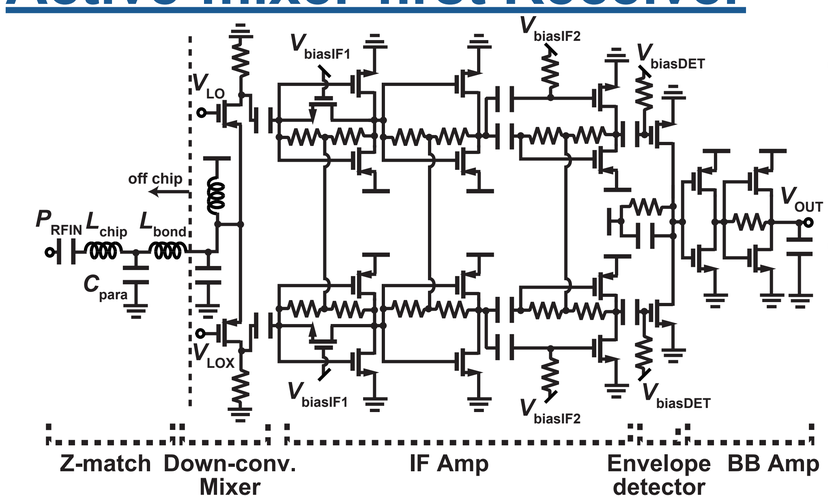
Ultra-Low-Power RF Transceiver[5]

0.5-V 5.8-GHz Transceiver



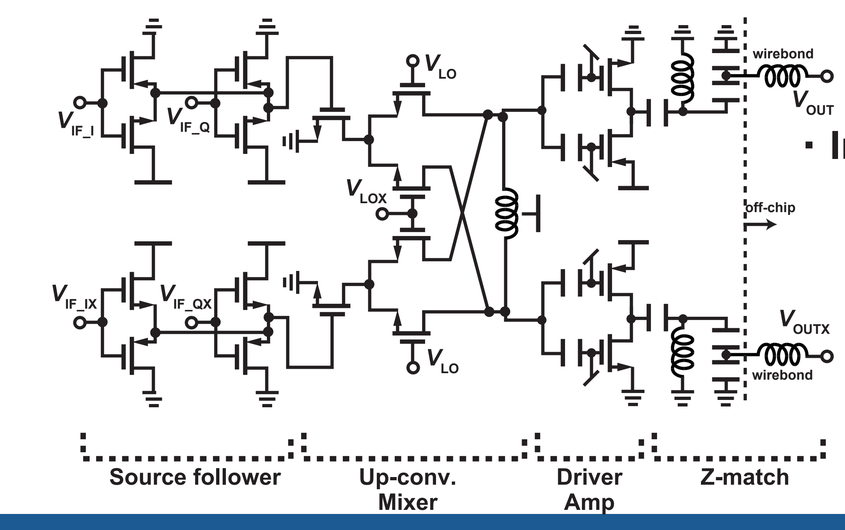
- 0.5V supply voltage
  - Foward Body Bias
- OOK Receiver
  - Low Power
- QPSK Transmitter
  - high datarate
- PLL using ILFD and Current-reuse VCO

Active-mixer-first Receiver



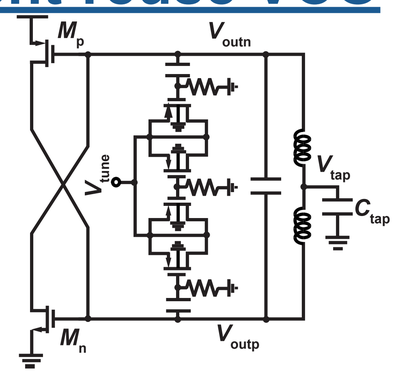
- Active-mixer-first
  - Low Power
  - Moderate sensitivity
- Uncertain-IF
  - Low power of LO (free-running Osc.)

Inverter-based Transmitter



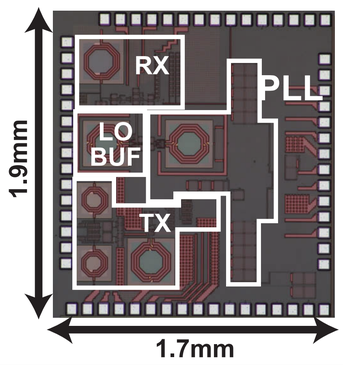
- Inverter-based DA
  - Reduction of Z-match ratio

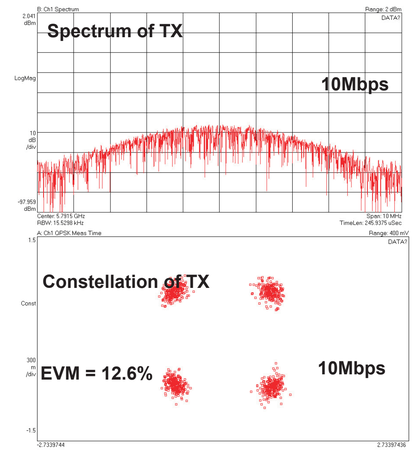
Current-reuse VCO

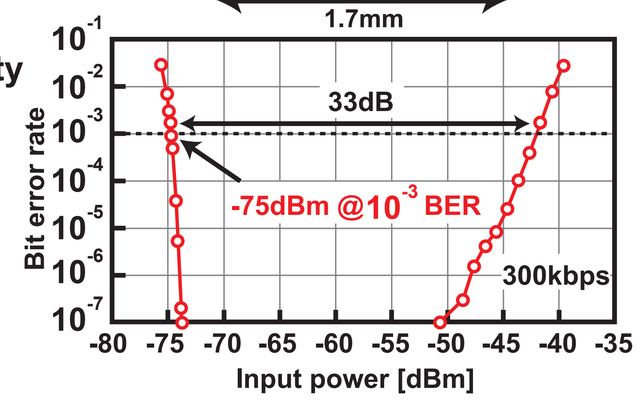


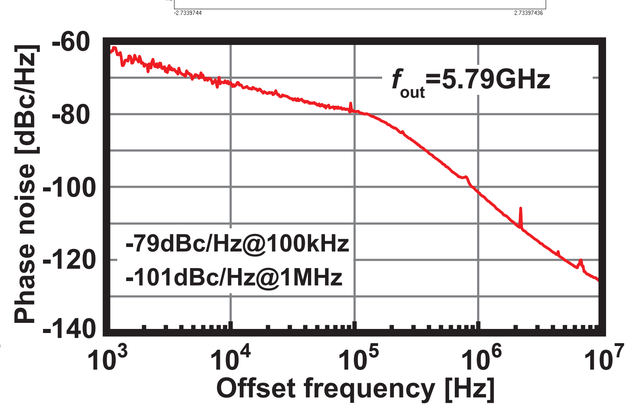
- Current-reuse VCO
- ☺ - Low Power
- ☹ - Amplitude-mismatch by its asymmetry
- Large capacitor for AC gnd
- ☺ -AC components of V_{outp} & V_{outn} are same

Measurement Results









	Supply voltage	Frequency	Modulation	Power	Sensitivity	Energy/bit
This work	0.5V	5.85GHz	OOK	830uW	-75dBm@300kbps	2.8 nJ/bit
JSSC 2013	0.5V	2GHz	OOK	52uW	-72dBm@100kbps	0.52 nJ/bit
VLSI 2010	0.65V	2.4MHz	BFSK	210uW	-86dBm@250kbps	0.84 nJ/bit

	Supply voltage	Frequency	Data Rate	Modulation	Power	Output Power	Energy/bit
This work	0.5V	5.79GHz	10Mbps	QPSK	2.86mW	- 31dBm	0.29 nJ/bit
VLSI 2010	0.65V	2.4GHz	1Mbps	BFSK	1.15mW	- 5.2dBm	1.15 nJ/bit
JSSC 2011	0.7V	920MHz	5Mbps	FSK	0.7mW	- 10dBm	0.14 nJ/bit

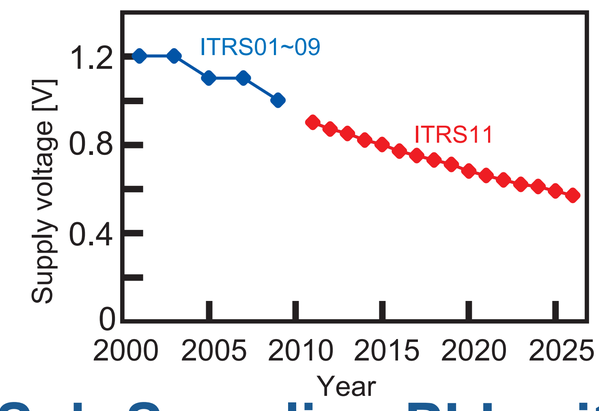
High operation frequency under low supply voltage

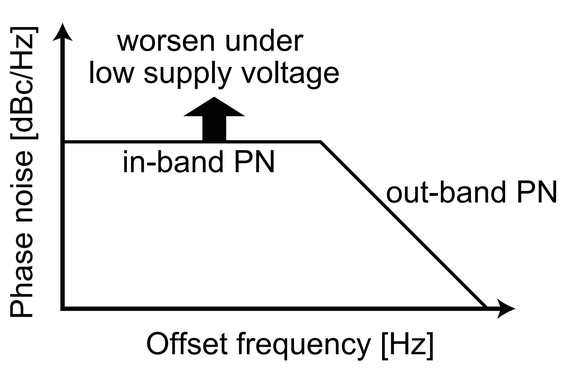
[5] S. Ikeda et al., RFIC, pp. 29-32, 2014

Low Noise Sub-Sampling PLL[6]

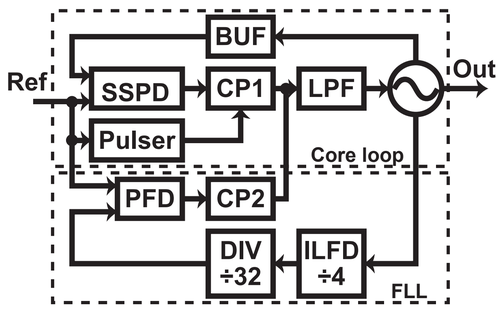
[6] S. Ikeda et al., A-SSCC, pp. 365-368, 2014

Motivation:Low voltage, Low phase noise PLL

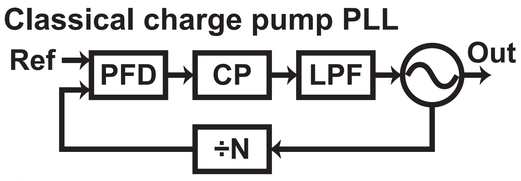




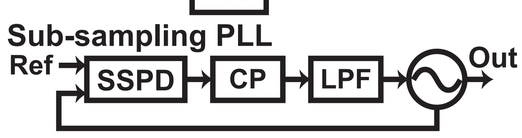
Sub-Sampling PLL with DtMOS



- Classical charge pump PLL



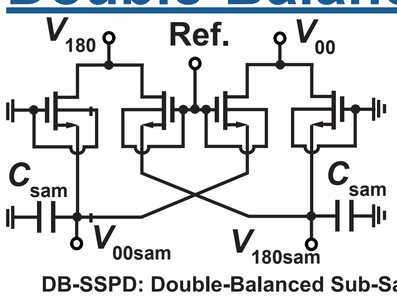
- Sub-sampling PLL

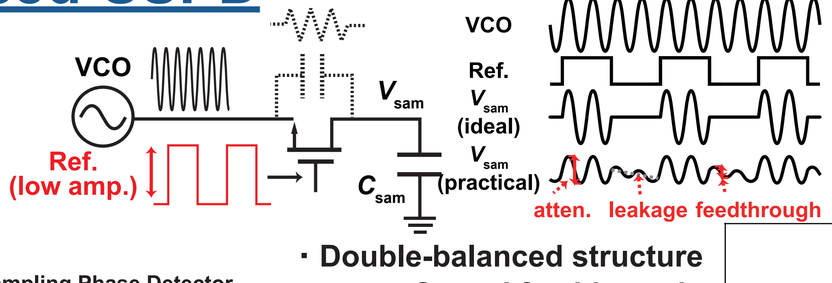


-Very low in-band phase noise

DTMOS: Dynamic threshold MOSFET

Double-Balanced-SSPD

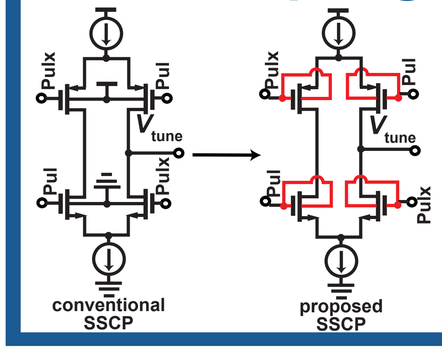


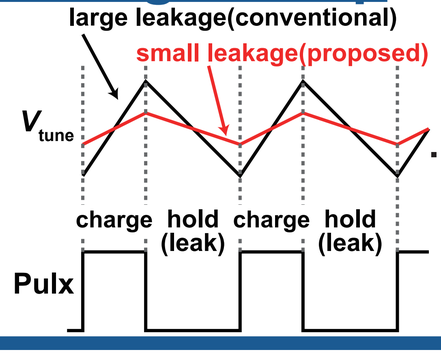


DB-SSPD: Double-Balanced Sub-Sampling Phase Detector

- Double-balanced structure
  -Cancel feedthrough

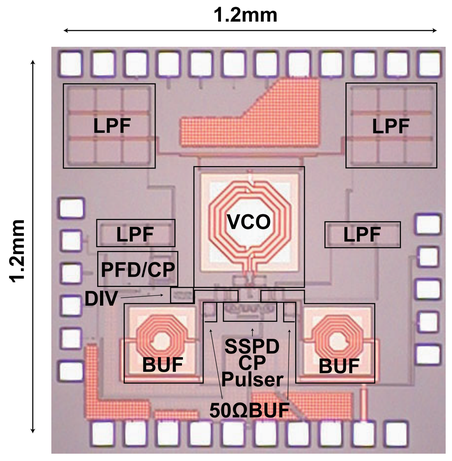
Sub-Sumpling Charge Pump



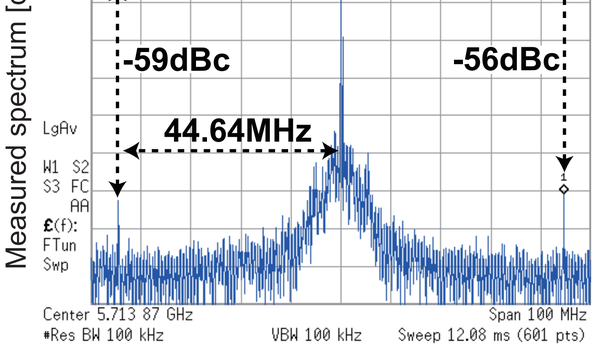


- DtMOS Switch
  -Low leakage CP

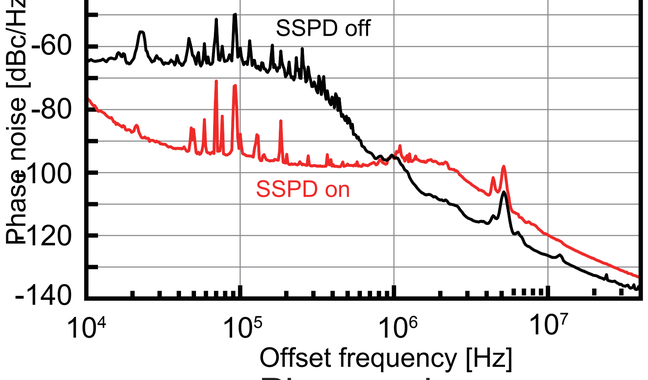
Measurement Results



Process	65 nm CMOS	
Supply voltage	0.52 V	
Input frequency (f_{ref})	44.64 MHz	
Output frequency (f_0)	5.71 GHz	
Phase noise	out-band (10 MHz)	in-band (410 kHz)
	-120 dBc/Hz	-98 dBc/Hz
Power consumption	1.72 mW	
	VCO and BUF: 0.60 mW SS core loop : 0.12 mW FLL : 1.00 mW	



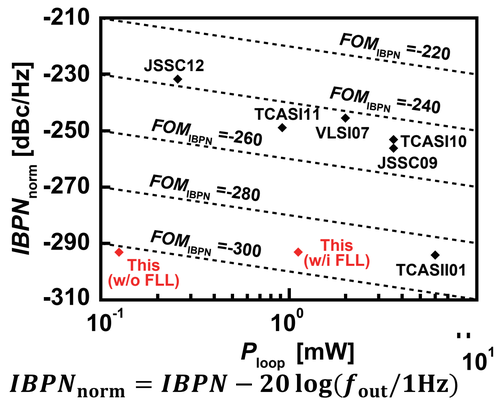
Output signal spectram



Phase noise

	Tech. [nm]	f_{out} [GHz]	V_{DD} [V]	PN(out-band) [dBc/Hz]	PN(in-band) [dBc/Hz]	Power [mW]
This work	65	5.71	0.52	-120@10MHz	-98@410kHz	1.72
JSSC12	130	0.433	0.5	-92@1MHz	-59@149kHz	0.44
TCASI11	90	2.24	0.5	-77@100kHz	-62@10kHz	2.1
TCASI10	180	2.56	0.6	-105@1MHz	-65@4kHz	14.4
VLSI07	180	1.9	0.5	-120@1MHz	-60@7kHz	4.5
JSSC09	90	2.59	0.5/0.65 (1)	-113@1MHz	-69@1kHz	6.0
TCASII01	130	9.12	0.5/0.8 (2)	-105@1MHz	-95@40kHz	12

(1)0.5V:Analog, 0.65: Digital supply,(2)0.5V: Analog, 0.8V: Digital supply



$$IBPN_{\mathrm{norm}} = IBPN - 20\log(f_{\mathrm{out}}/1\mathrm{Hz})$$

$$FOM_{\mathrm{IBPN}} = IBPN_{\mathrm{norm}} + 10\log(P_{\mathrm{loop}}/1\mathrm{mW})$$

Low phase noise and good power comsumption